FAC 2009 – Grenoble

Pierluigi Daglio
AMS Center of Competence

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AMS Macrocells Verification Today in a Challenging Industrial Environment. Status, Activities and Trends.

Marco Carlini – Pierluigi Daglio
AMS Center of Competence

Pier Luigi Rolandi
AMS & RF Design Flows Director

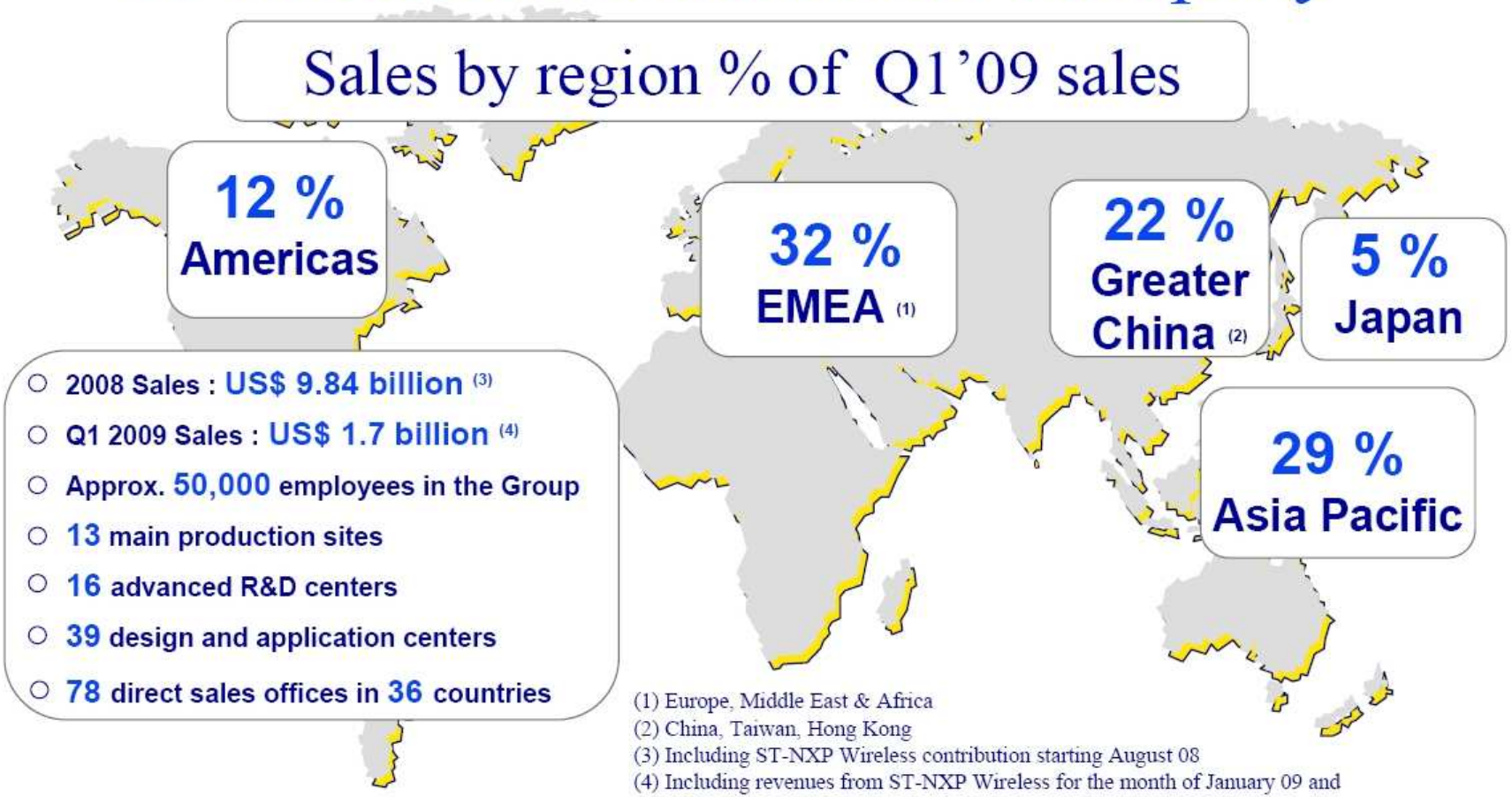
STMicroelectronics Mission

To offer strategic independence to our partners worldwide, as a profitable and viable broad range semiconductor supplier

Company Overview

A Global Semiconductor Company

Sales by region % of Q1'09 sales



- 2008 Sales : US$ 9.84 billion (3)
- Q1 2009 Sales : US$ 1.7 billion (4)
- Approx. 50,000 employees in the Group
- 13 main production sites
- 16 advanced R&D centers
- 39 design and application centers
- 78 direct sales offices in 36 countries

(1) Europe, Middle East & Africa
(2) China, Taiwan, Hong Kong
(3) Including ST-NXP Wireless contribution starting August 08
(4) Including revenues from ST-NXP Wireless for the month of January 09 and ST-Ericsson starting February 09

A Few Words About Agrate AMS Team

- **AMS Design Flow & Simulation**
- **Statistical Analysis & Design Centering**
- **AMS Innovative Verification Techniques**

A Few Words About Agrate AMS Team

AMS Design Flow & Simulation

- AMS design flow definition, validation, deployment and support to customers
- Exhaustive fast-spice engines benchmarking activity
- Cosimulation methodology definition, validation, deployment and support
- AMS design environment development and deployment to divisions
- Drive and interact with major EDA vendors and start-up companies

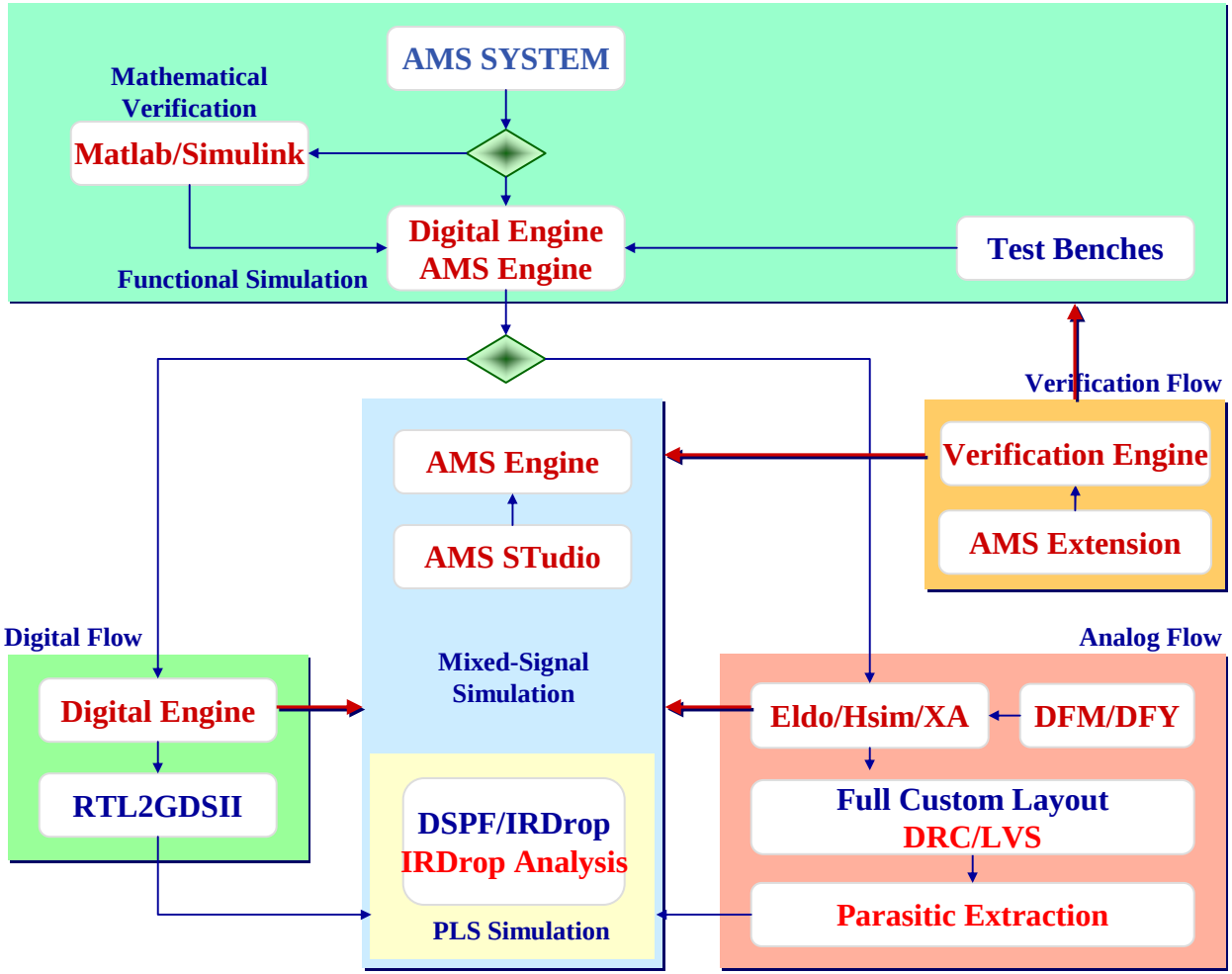
Statistical Analysis & Design Centering

- DFM & DFY simulation and modelling based flows deployment and support
- Benchmarking new solutions available on the market
- Internal and external customers training and support
- Advanced methodologies for the automatic regression of analog IPs
- Automatic generation of analog IPs documentation

AMS Innovative Verification Techniques

- Verification plans released for several AMS macrocells as service activity
- Collaboration with major EDA vendors about AMS verification
- AMS verification methodologies in use or under investigations
  - Constraint Random Verification (CRV) – Specman based environment
  - Coverage Driven Verification (CDV) – Specman based environment
  - Assertion Based Verification (ABV) – SystemVerilog works in progress
  - Analog Formal Verification (AFV) – Future works with Synopsys, Mentor & Verimag
- Analog waveforms automatic regression flow implemented and deployed
- Best practices documents released to divisions
- Examples of model validation and IP verification services already done
  - SRAM model validation with IP at transistor level and model in Verilog
  - IP transistor level validation with test-benches in Verilog-A
  - IP HDL model coverage with IP in VHDL and test-benches in Specman e-language

Smart Design Flow for AMS Applications



Additional Verification Tools

- Circuit Check
- A.R.A.W.

2008

New Supported Tools

- XA-NCSim
- PT2SPICE
- D.O.E.

2009

AMS Extension To Verification

AMS dynamic functional verification

- A simulation based activity **on the critical path** towards chip robustness and first silicon success
- Committed to provide
  - AMS IPs verification services to designer community
  - Research and benchmarking of innovative solutions

Explorations, Progresses & Roadmap

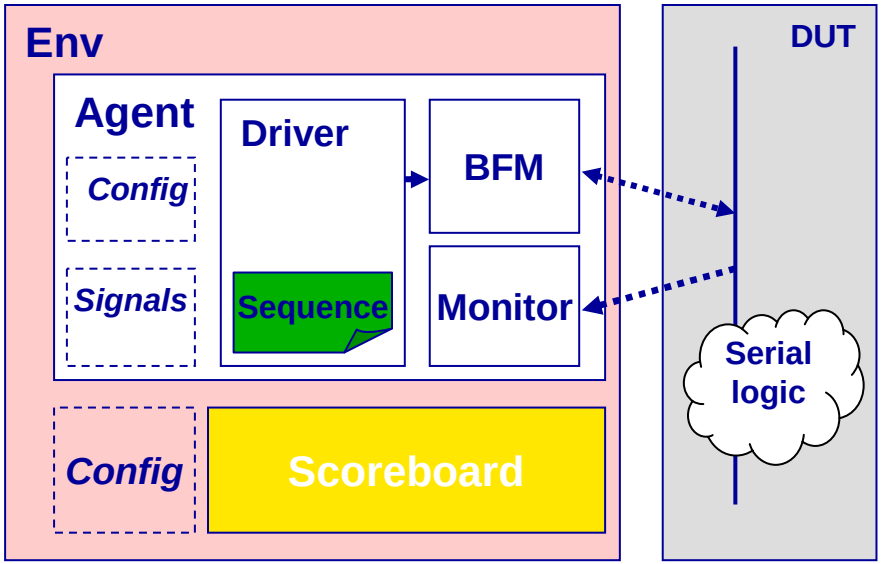
- 2007 - Yogitech AMSvKit integration in our smart AMS flow
- 2008 – Specman deeply analyzed and **e-language** verification
- 2009 - System Verilog within OVM & VMM
- 2010 – Analog Formal Verification
- 2011 – Direct simulation from executable specifications

Specman Based AMS Verification

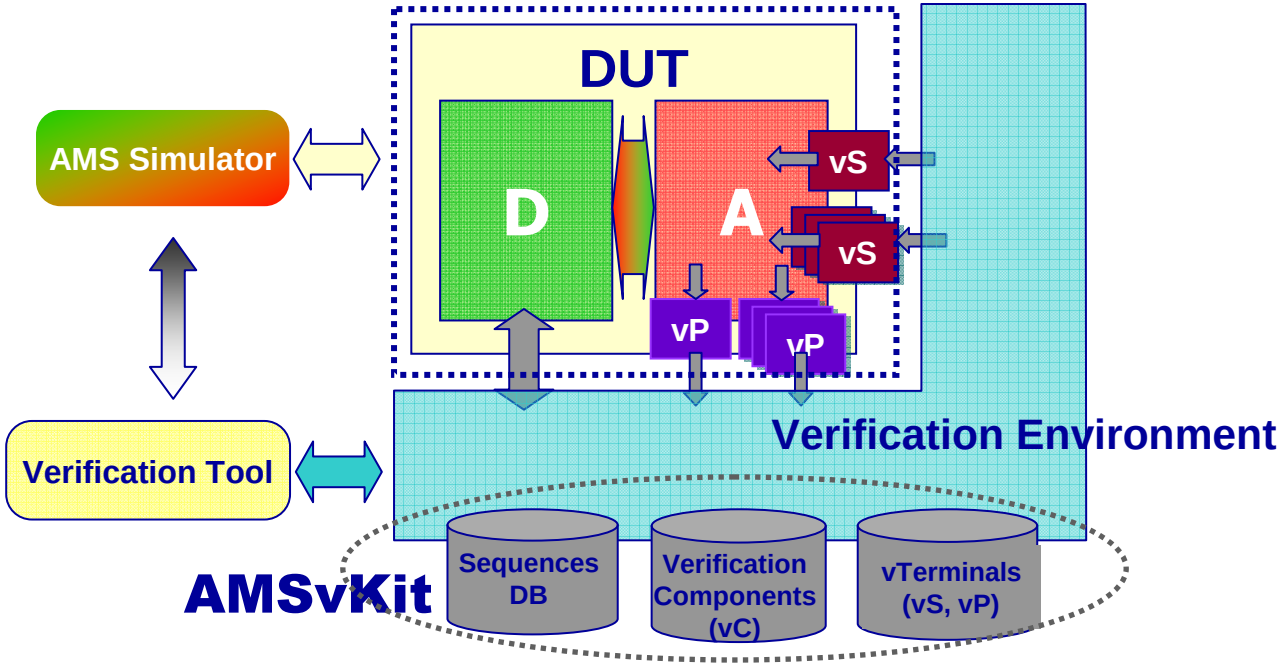
- **Specman** is the tool/compiler/debugger for *e* language
  - *Constraint Based/Random Generation, Checking and Coverage*

Coverage Driven Verification	=	Automatic Generation	+	Coverage Measurement

- eVC development
  - Verification plan
  - Verification components
- Verification environment
  - Model vs Scoreboard
  - RTL vs Scoreboard
  - RTL vs Model *(validation)*



Yogitech AMSvKit AMS Extension



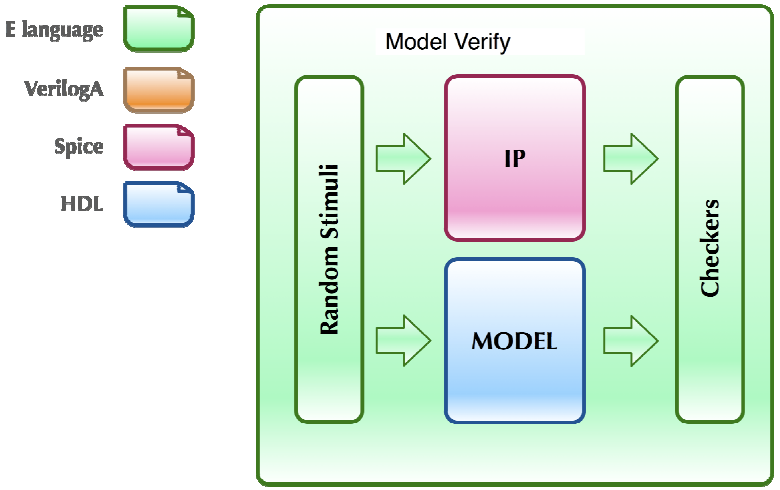
- **Extending digital verification methodology to the analog domain**
- **Integrating verification tools and mixed-signal simulators**
- **Using eVC block libraries to interface the two domains**

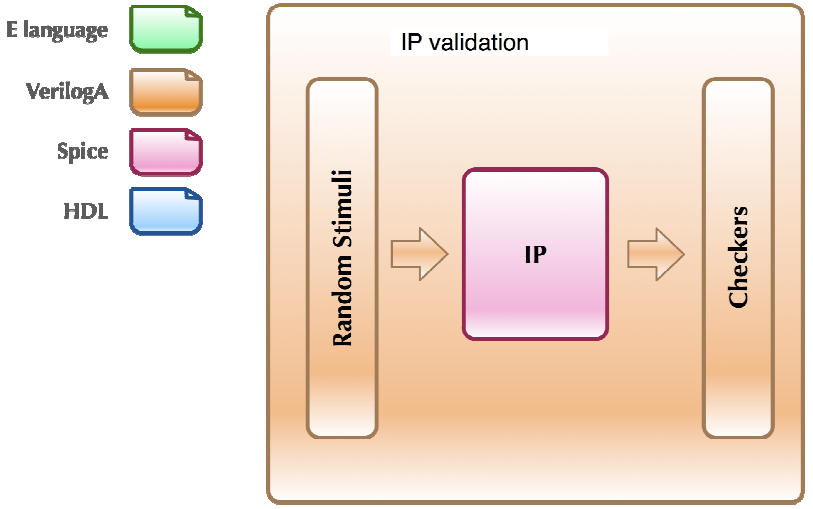
Verification Calls for Automation

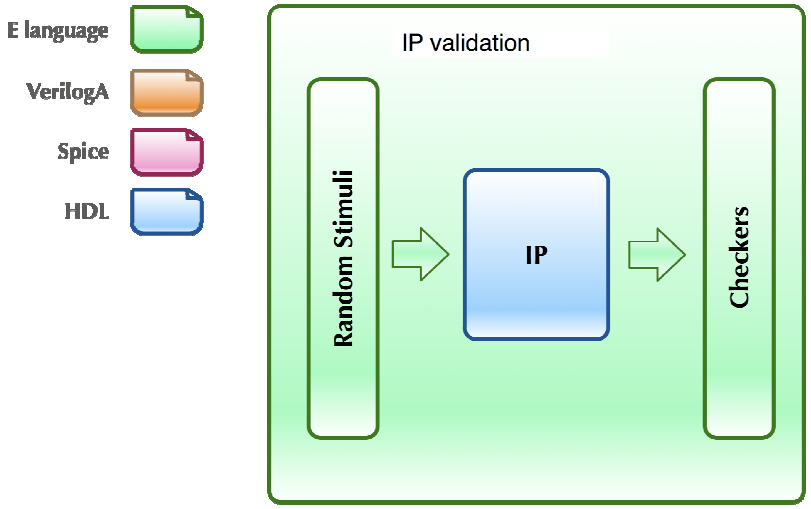
"I can remember the exact instant when I realized that a large part of my life from then on was going to be spent in finding mistakes in my own programs"

M.Wilker, Cambridge Labs 1949

IP Validation Services Provided to Divisions







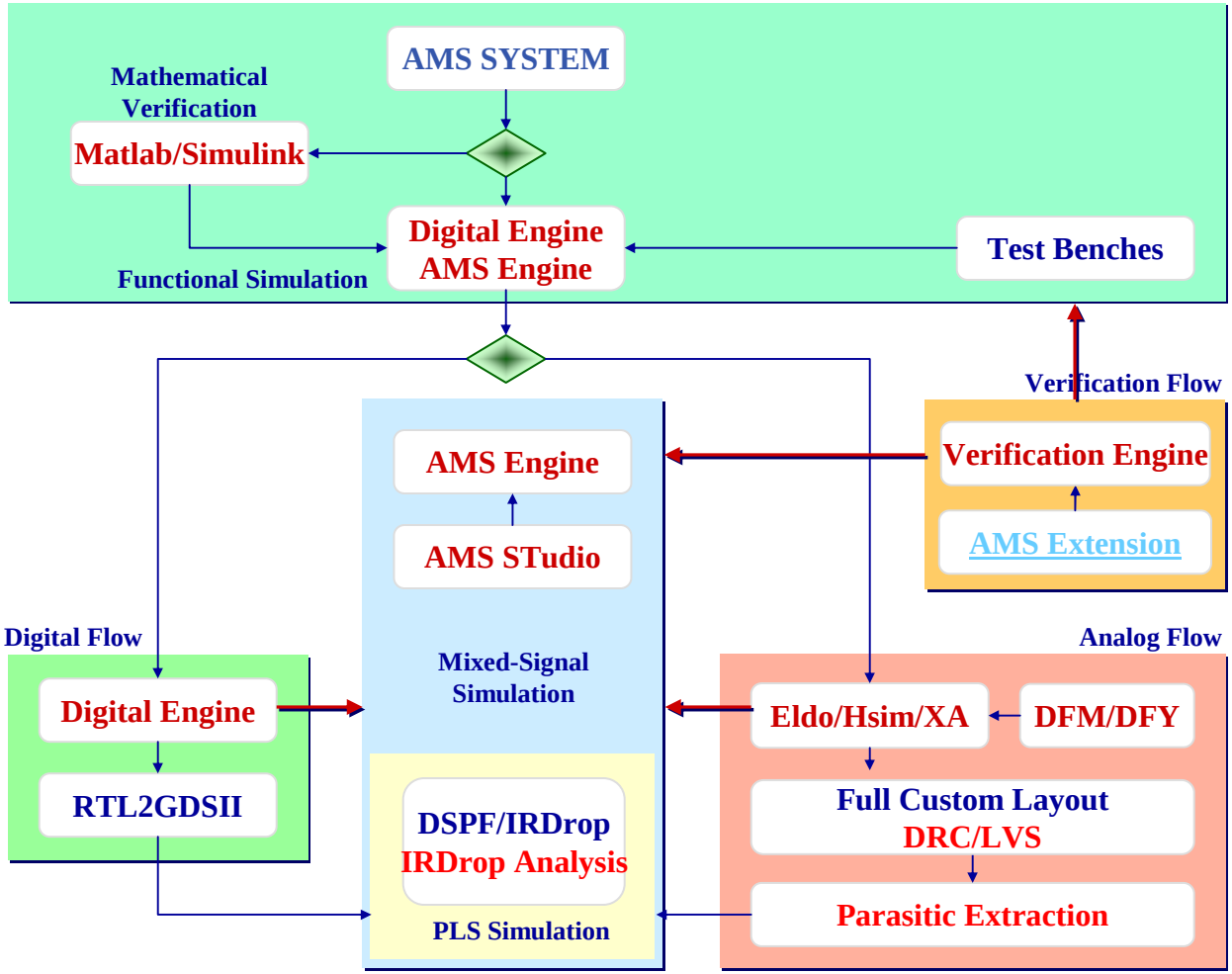
Three examples of IP validation services

- ✓ SRAM Model Validation – HSIM-NCSim
- ✓ IP transistor level validation – HSIM and XA
- ✓ IP HDL model coverage - NCSim

Automated Regression for Analog Waveforms

- **A.R.A.W. flow**
  - Wave View Analyzer + Command Environment (ACE) + PERL or TCL scripts
  - Real break-through in analog waveforms checking solution
    - From two weeks to half an hour to check 200 analog waveforms of a flash memory
    - Sign-off reports automatically generated for design managers
    - Need to improve benefit awareness, marketing activity and training set up
    - Sensible reduction of the risk of silicon failure
    - PERL or TCL aware engineer needed to write down the check plans

Smart Design Flow for AMS Applications



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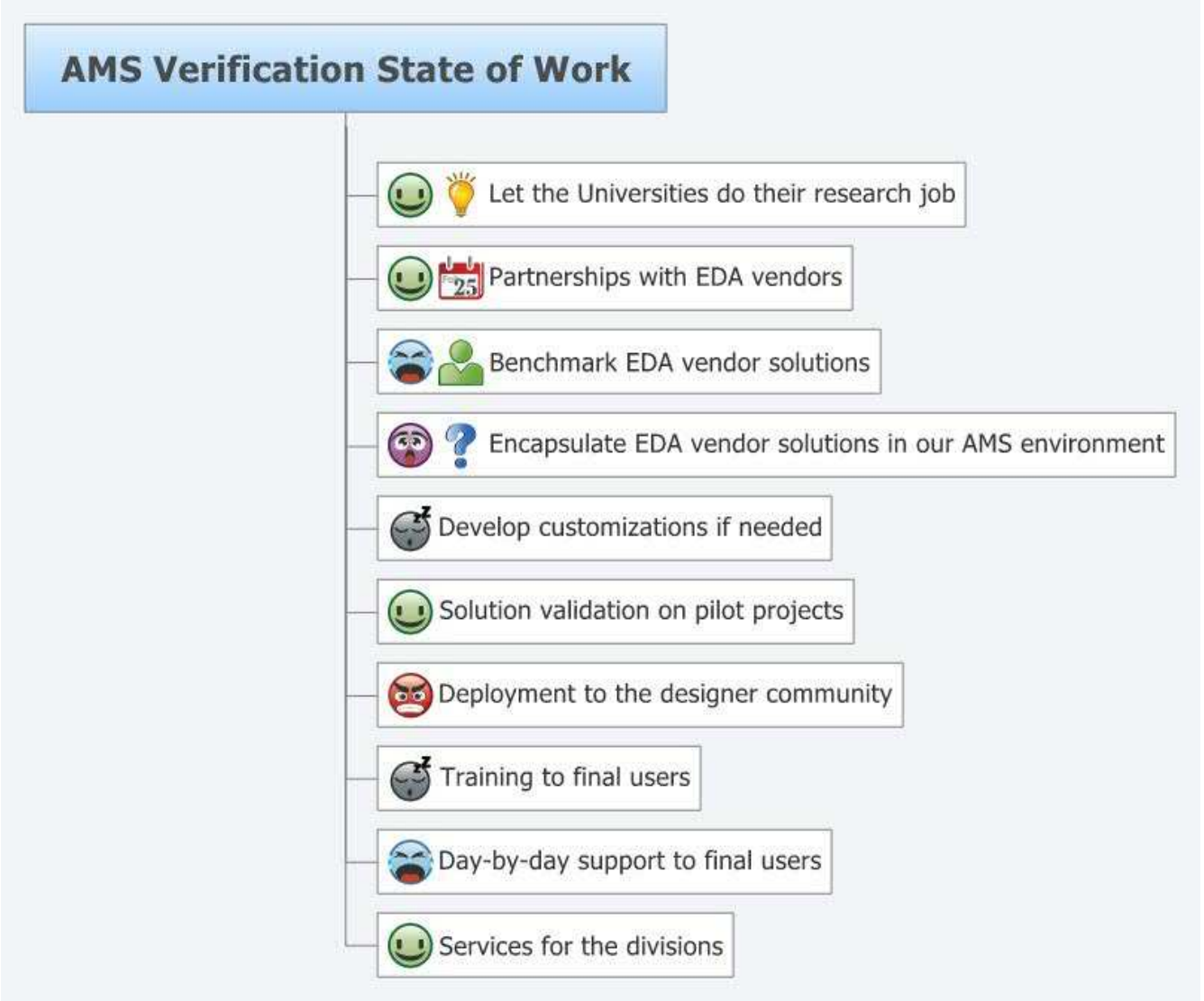
AMS Verification State of Work



Conclusions – The Key Points

- AMS verification techniques start now to be used in companies
- Mainly confined to Constraint Random Verification approach
- Assertion Based Verification approach under deep investigations
  - Collaborations started with major EDA vendors
  - First applications foreseen in 2009 & 2010
- Analog Formal Verification seems still far from being used
  - Ready to set up collaborations with EDA vendors & research institutes
  - Interest from a commercial point of view is mandatory to speed up
  - Early contacts with some players (Mentor & Verimag)
  - Thesis students availability will boost the familiarization
- Key points
  - Deeper interactions with Cadence, Mentor & Synopsys to steer proper activities on advanced AMS verification
  - Enhance the manager awareness in AMS verification and functional coverage advantages
  - Create an AMS verification culture
  - Design groups need a verification engineer in their ranks

Conclusions – The Three Players

- **Universities & Research Institutes**
  - Insist on the research on Analog Formal Verification
  - Invest in human resources
  - Not being too much disconnected from industries
  - Send thesis and PHD students to companies for stages
  - Promote their researches and give program prototypes to EDA vendors and companies
  - Not being confined as academic world
- **EDA Vendors**
  - Invest in AMS verification and Analog Formal Verification even if R.O.I. is not seen as immediate
  - More collaborations with Universities & Research Institutes
  - Create standard approaches and not one different methodology for any vendors
  - Increase collaborations and joint ventures with semiconductor companies
  - Believe in these techniques as a break-through for the future AMS designs
- **Semiconductor Companies**
  - Invest more resources in internal CR&D groups
  - Create and push the AMS verification culture at manager level
  - Spend in verification tools and solutions
  - Accept students from Universities & Research Institutes on AMS verification
  - Strongly collaborate with EDA vendors giving detailed specifications for the AMS verification tools
  - Setup well defined collaboration programs in terms of resources, time scheduling and final result utilization

THANK YOU !!!

AMS Center of Competence

pierluigi.daglio@st.com
marco.carlini@st.com