Verifying Analog Designs: Needs, Constraints and Future Challenges for Complex Analog Designs from Cells to System

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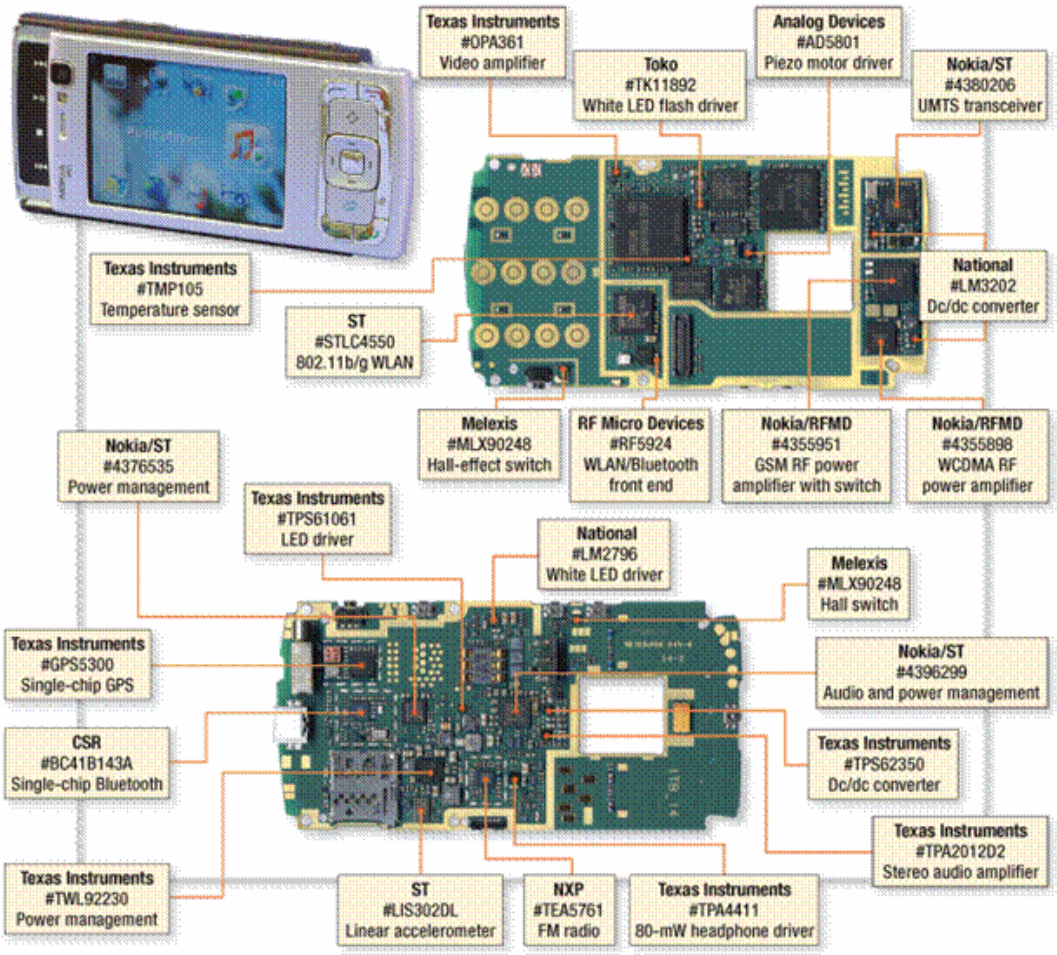
Outlook

- **Analog design context**
- **Cell design paradigm going below 65nm**
- **SoC design paradigm going below 65nm**
- **R&D Directions**

Analog design context

AMS IC's define today's killer products

- **Most eye-catching features are supported by A/M-S IC's**
  - **Transceivers**
    - **GSM**
    - **W-CDMA**
    - **Bluetooth**
    - **WLAN**
    - **UMTS**
    - **WiFi**
  - **DC/DC converters**
  - **Power management IC's**
  - **A/V amplifiers**
  - **Power amplifiers**
  - **LCD drivers**
  - **Motor driver**
  - **FM radio**
  - **Sensors**
  - **Flash memory**
  - **etc**



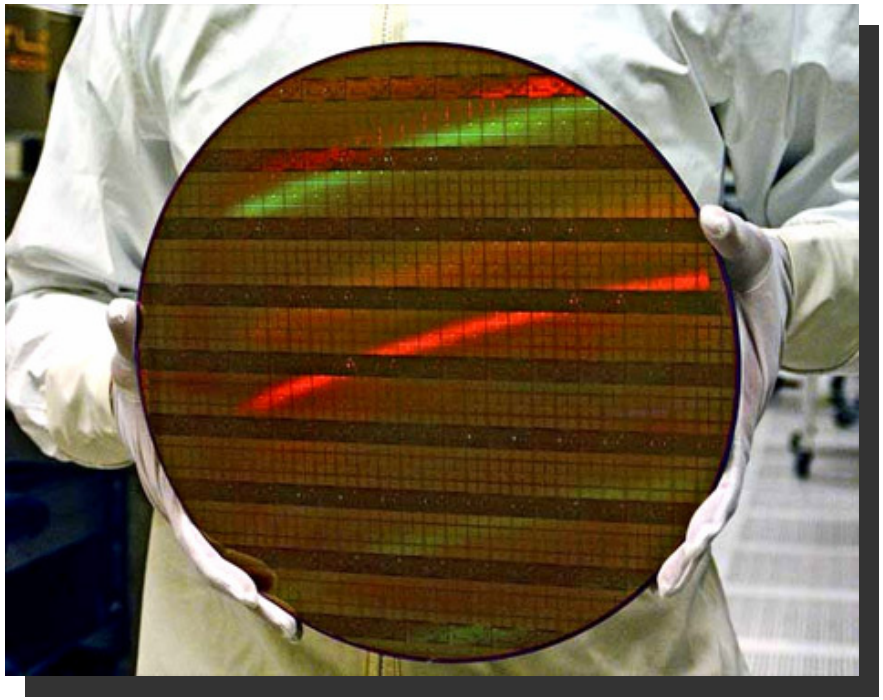
Problems with AMS SoC Verification

- **Those who develop AMS SoC have 3 concerns which prevent them from sleeping well :**

Will it be functionally correct ?

Will it be robust ?

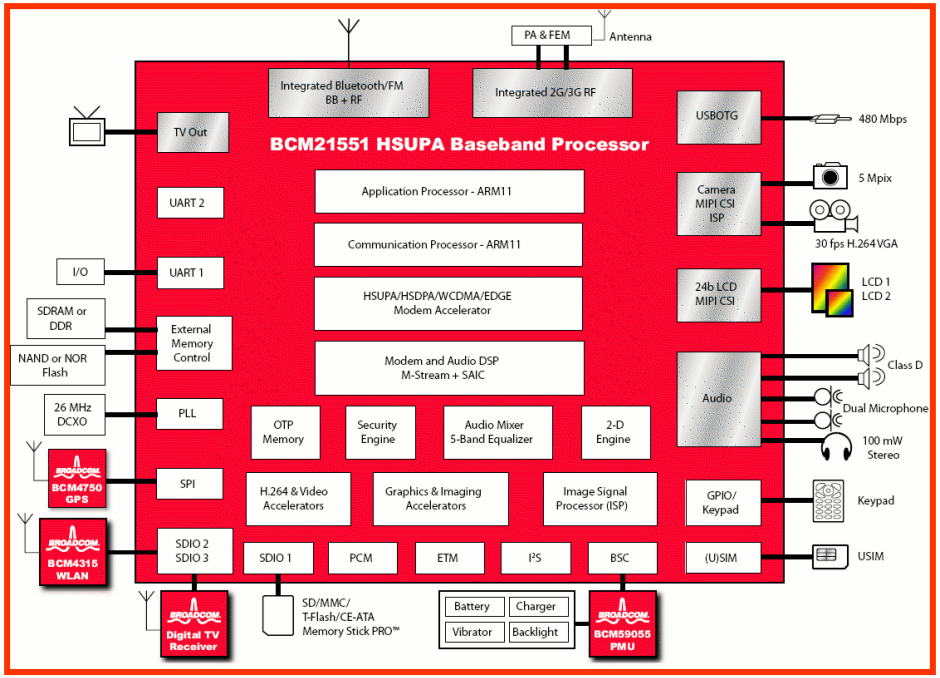
Will it be reliable ?



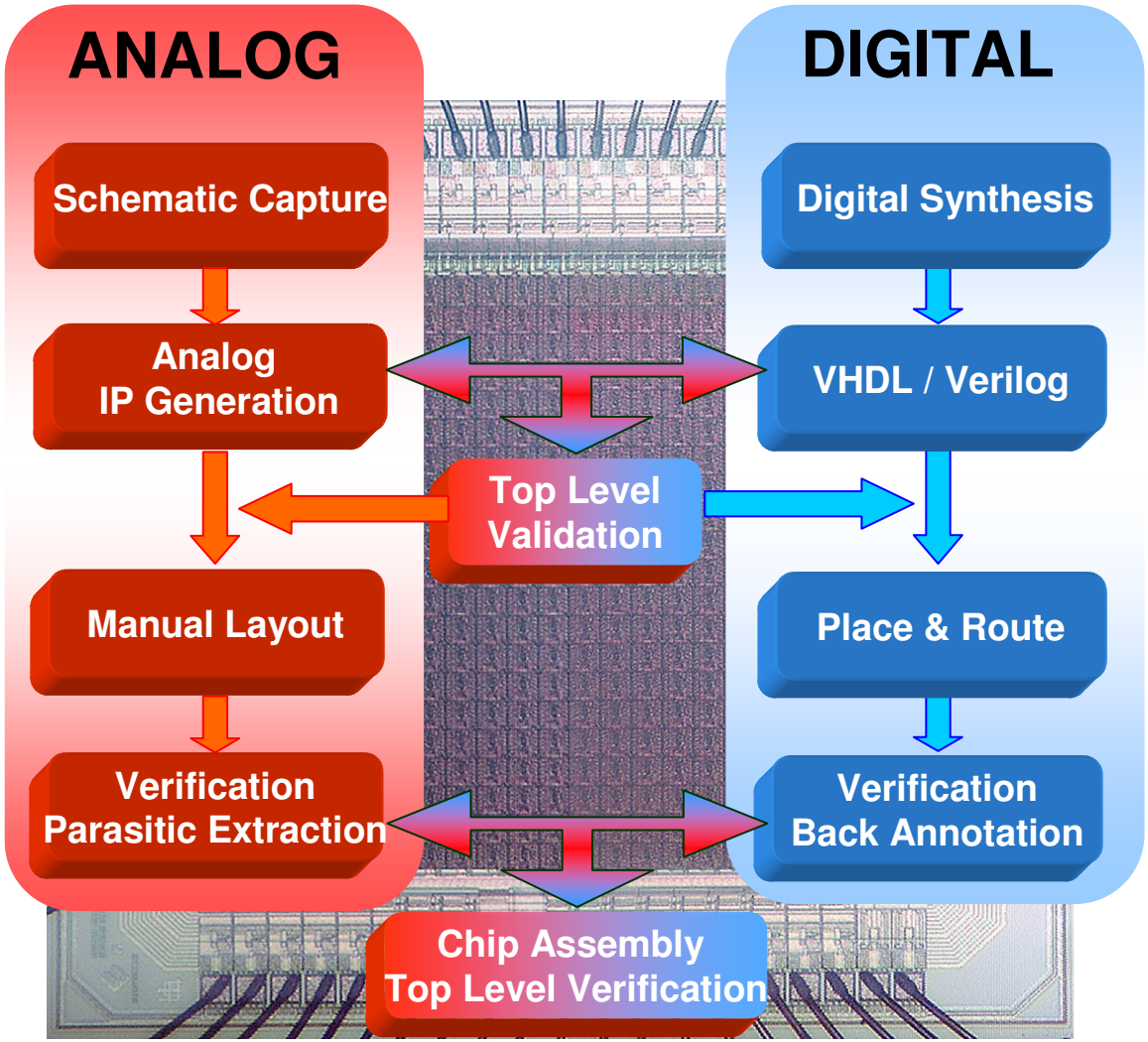
Will it be functional ?

- **The end customer is waiting for a <u>working</u> prototype**

- **Challenge : assemble and verify, in less than one month :**
  - Analog/RF cells
  - 3rd-party HDL IP blocks
  - Embedded RAM
  - Custom logic
  - SV testbench



AMS vs. Digital Design Flows

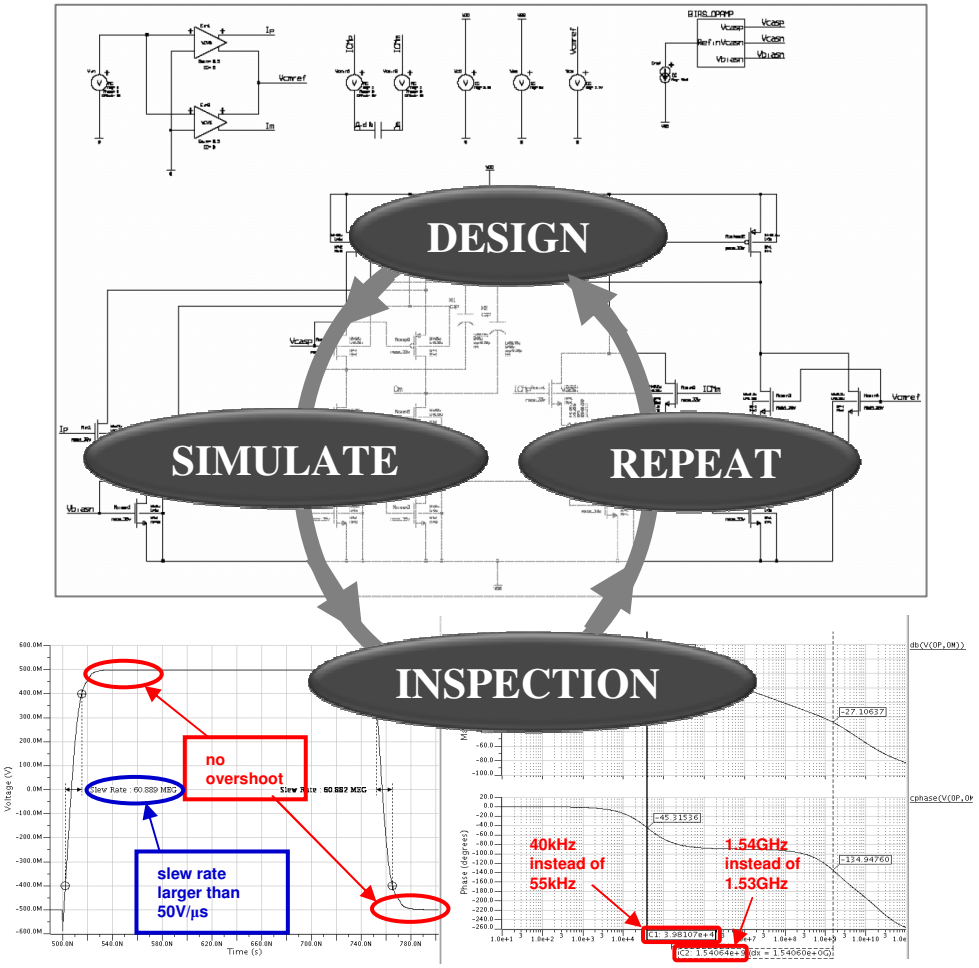


- Analog designers are facing several bottlenecks
  - No automation available in
    - Synthesis
    - P&R
    - Formal verification
- Increased complexity:
  - Smaller geometries of sub-micron processes allows bigger designs with more functionalities
- Increased process variability:
  - Dramatically critical in sub-micron processes
- TTM is under pressure
- Consequence: Analog designer must increase productivity in
  - Cell design
  - System validation

Cell design paradigm going below 65nm

Analog Cell Functional Verification

- **Nominal**
  - SPICE simulations
  - Waveform inspection
  - Scripting
- **Worst case**
  - Voltage and temperature variations
  - Process Corners



More Complex Simulations

- Systems becoming more complex require complex AMS cells with more functionalities
- Nanometer processes have more effects (stress, dispersion …) that make design phase more complex.
- Analog IP validation requires post layout simulation for accuracy
  - Reduction algorithms becoming critical
- Analog IP validation cannot be done anymore with corner-based simulations
- Simulations getting more complex with Digital/Analog/RF interactions

Increasing Number of Simulations

- Because of all possible configurations, a huge number of simulations has to be managed
  - For example, LDO regulator characterization: 41,000 simulations during 1 week.
- Possibility to improve design productivity with a simulation manager
  - Netlist creation
  - Simulation launch and distribution over the network
  - Results post processing with Pass/Fail flags
  - Results synthesis in documentation
- MGC proposing a simulation manager tool (ICanalyst)
  - Same LDO example takes now ½ day

Monte Carlo Simulation

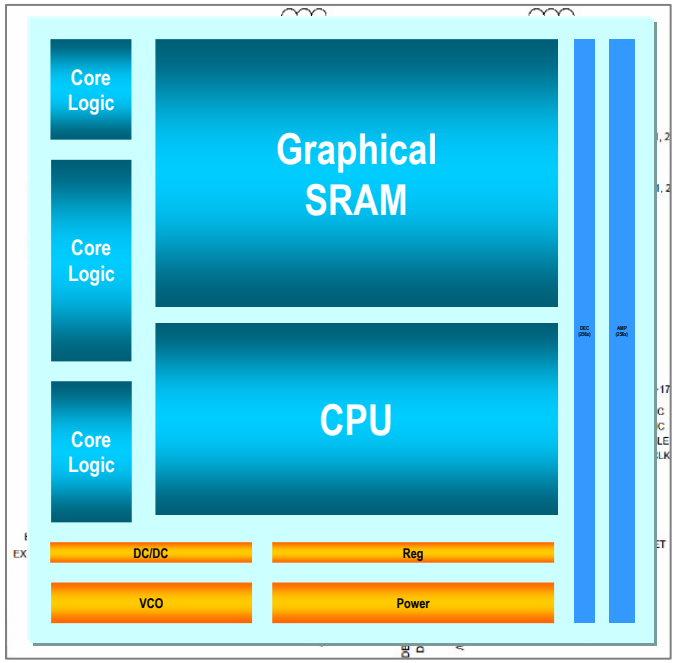
- **Monte-Carlo simulations are needed but simulation time explodes**
  - **100's of runs gives a rough guess on results**
  - **20,000's runs needed for guaranteed tight accuracy**
  - **Solution 1: Enhance MonteCarlo (proposed by MGC in ICanalyst & soon in Eldo)**
    - **QMC suites accelerate convergence (break $N^{-1/2}$ rate)**
    - **Adaptive MC stops when prescribed accuracy is obtained**
    - **Incremental MC allows continuation of MC simulation (add more runs)**
  - **Solution 2: Modeling can be used for simple problems without discontinuity**
    - **Simulate sampled points to create a performance model**
    - **Run MC on the model**
    - **Can decrease the simulation time and get very accurate results with 20 000 (fast) MC runs from a model based on 100/150 simulations**

SoC design paradigm going below 65nm

Approaches to AMS Verification

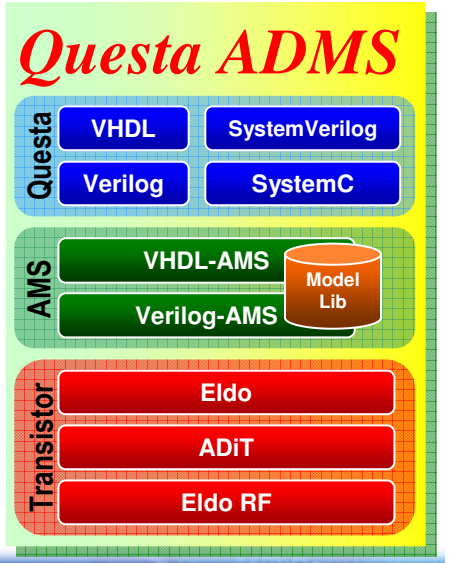
- **Tightly linked analog + digital functions make system-level simulation mandatory**

- **Most frequent Mixed-Signal SoC errors are integration errors**
  - Interconnect
  - Transposed buses
  - Control signals inverted
  - Un-tested operating modes
  - Multiple power domains

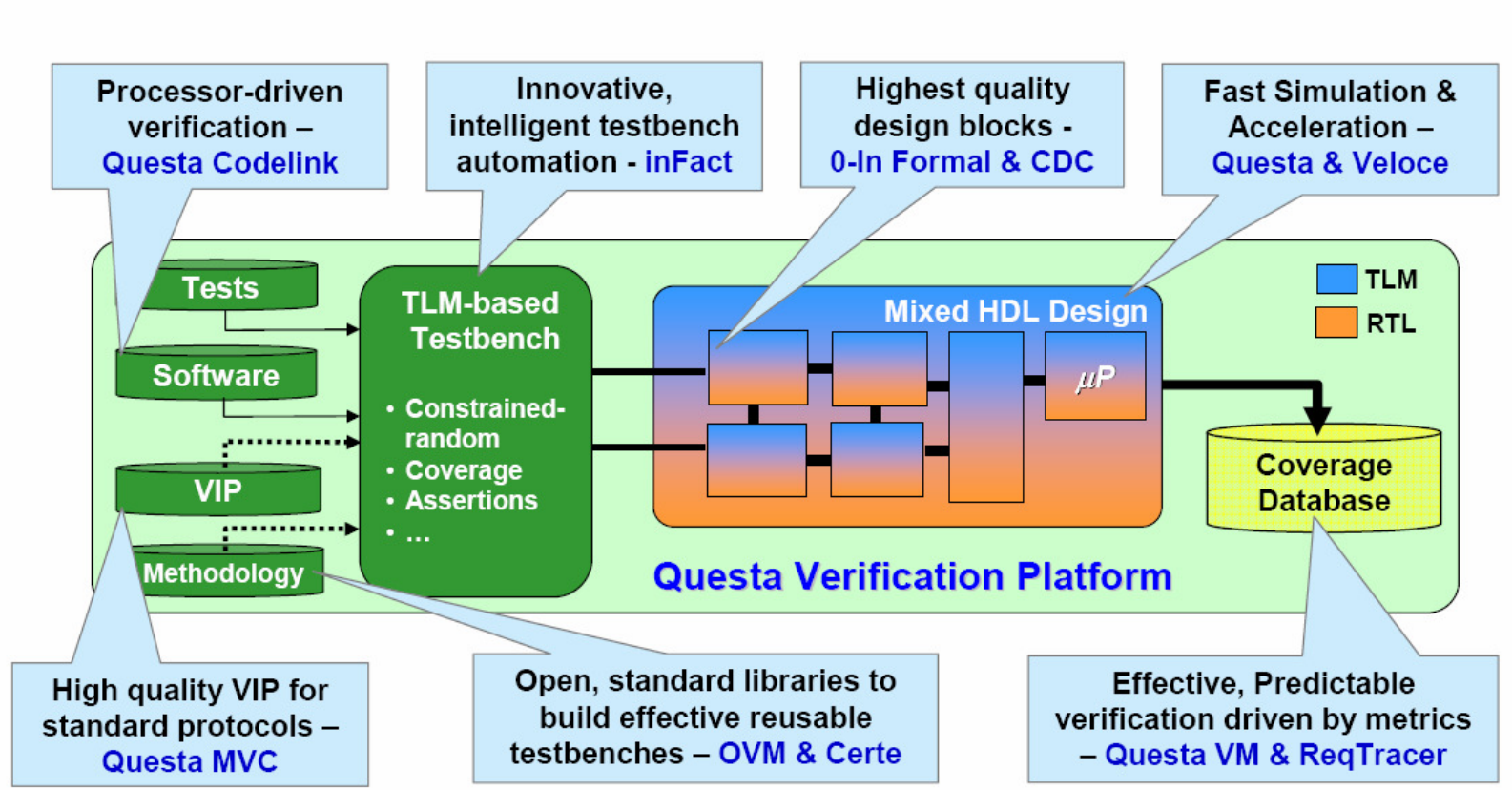


Problems to solve

- AMS SoC represents today multi-million transistors IC's with possibly few million analog
- Analog blocks representation is an issue:
  - Transistor → capacity problem, even with Fast-SPICE, makes simulation too slow
  - VHDL-AMS → investment in modeling needed, and still a little slow
  - VHDL-RN → equivalent in modeling investment, cannot capture all analog effects, simulate faster (pure digital simulation)
  - Solution: Checkerboard methodology to use the best accuracy compromise depending on which part of the design is activated by the test vector
    - Critical cells: SPICE or Fast-SPICE
    - Interacting cells: VHDL-AMS
    - Inactive cells : VHDL-RN or "level 0" VHDL-AMS
    - This is the solution developped by MGC (Questa ADMS)



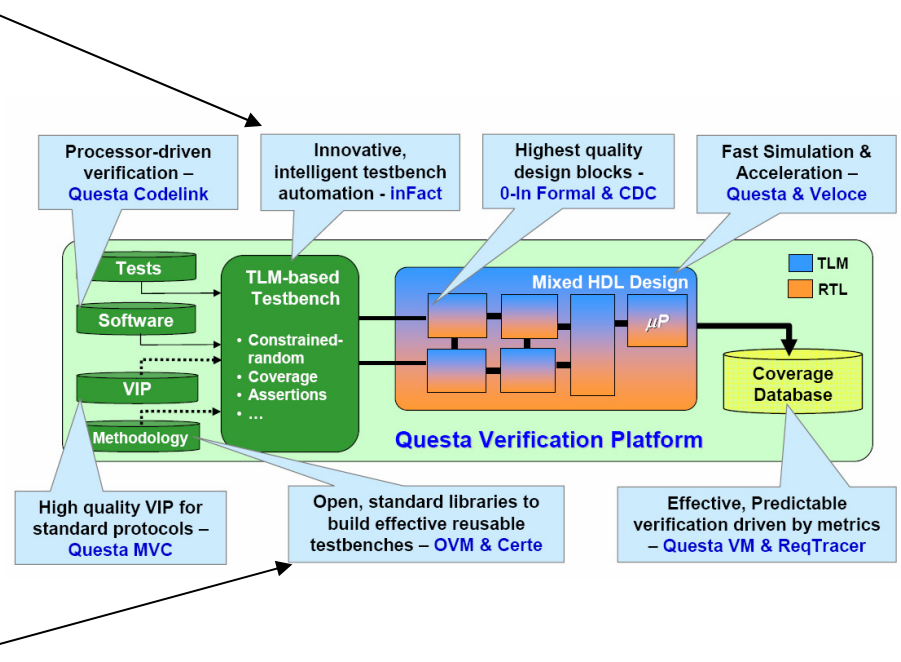
Digital SoC validations



- Not just a digital simulator
- Complete set of methodologies is needed

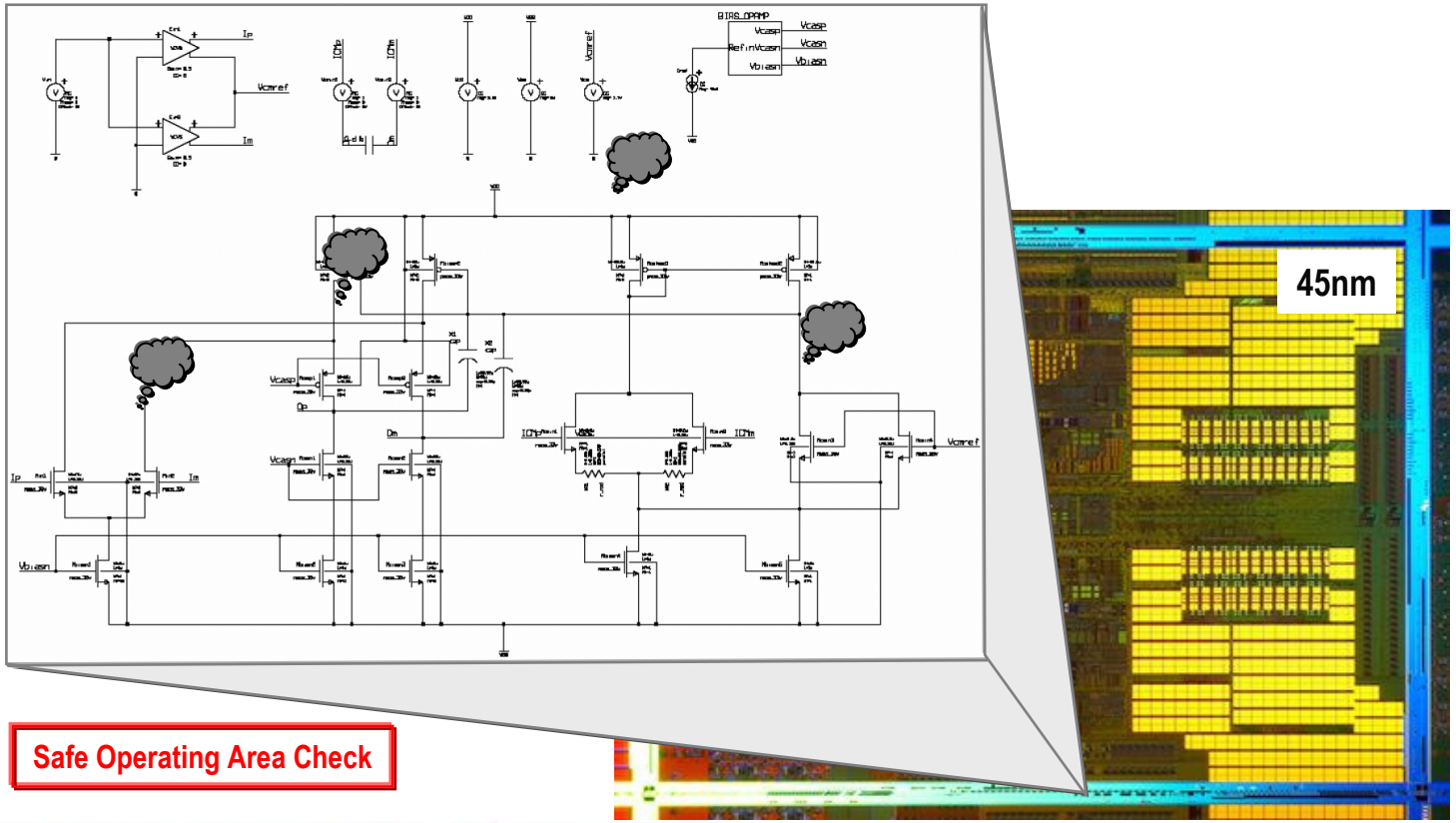
Needs for AMS SoC validations

- Need to transpose some digital techniques to AMS design
  - Test Bench Automation
    - Access advanced SPICE components in the digital testbench as behavioral models:
      - PWL source
      - Loads
      - Measurement checkers
  - OVM/SVA: need for a SVA Analog
    - Participation in Accelera standardization committee
      - Absolute time definition
      - Result comparison including tolerance



Assertions and Safe Operating Area

- ABV (Assertion Based Verifications) detects bugs at the source, saving valuable debug time
- Analog designers use SOA to detect malfunctions
- Dynamic assertion technology for mixed-signal



R&D Directions

Conclusion

- Analog IP design needs productivity improvement in both cell design and SoC validation
- Process below 65nm remove capacity/functionality bottleneck but opens design complexity/validation issues
- R&D directions
  - Statistical simulation
  - Full SoC formal validation (ABV, SVA-A)
  - Simulation time speed-up
    - More efficient algorithms
    - Multi-threading