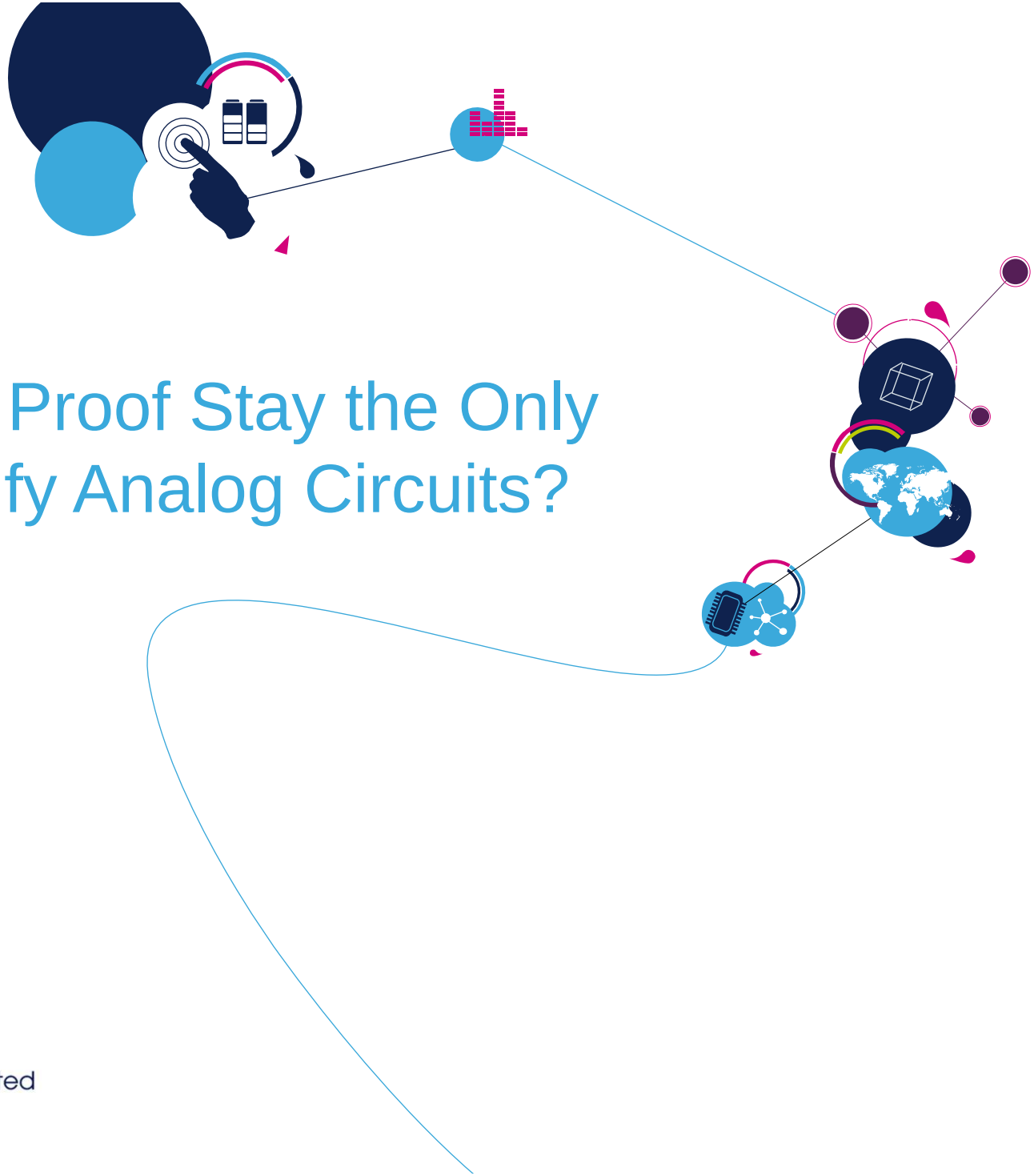

Will Silicon Proof Stay the Only Way to Verify Analog Circuits?

Pierre Dautriche

Jean-Paul Morin

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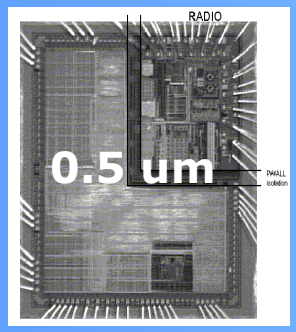
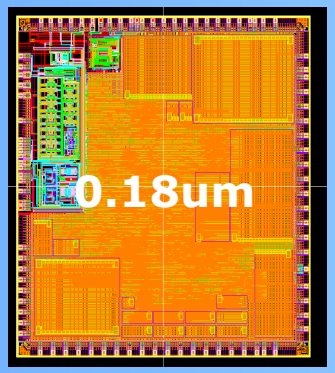
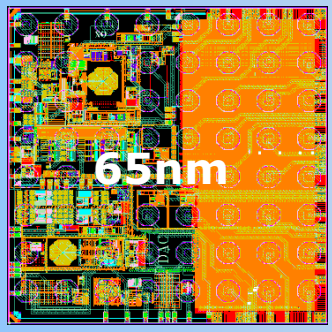
Advanced CMOS and analog ….

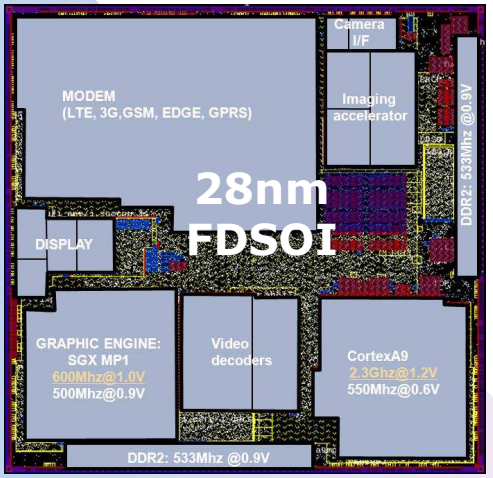
Embedded analog

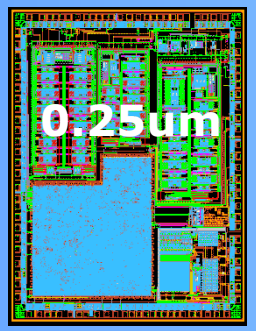
Embedded RF

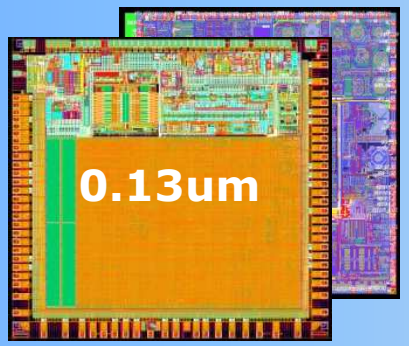


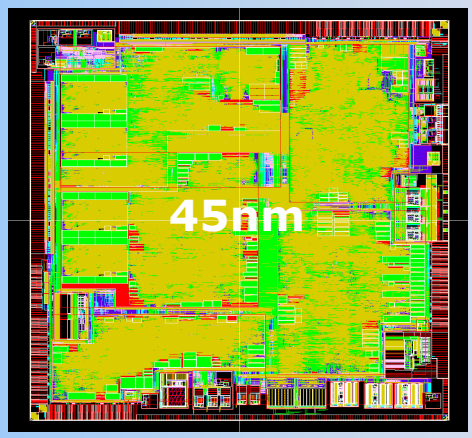












1997 2001 2005 2009 2013

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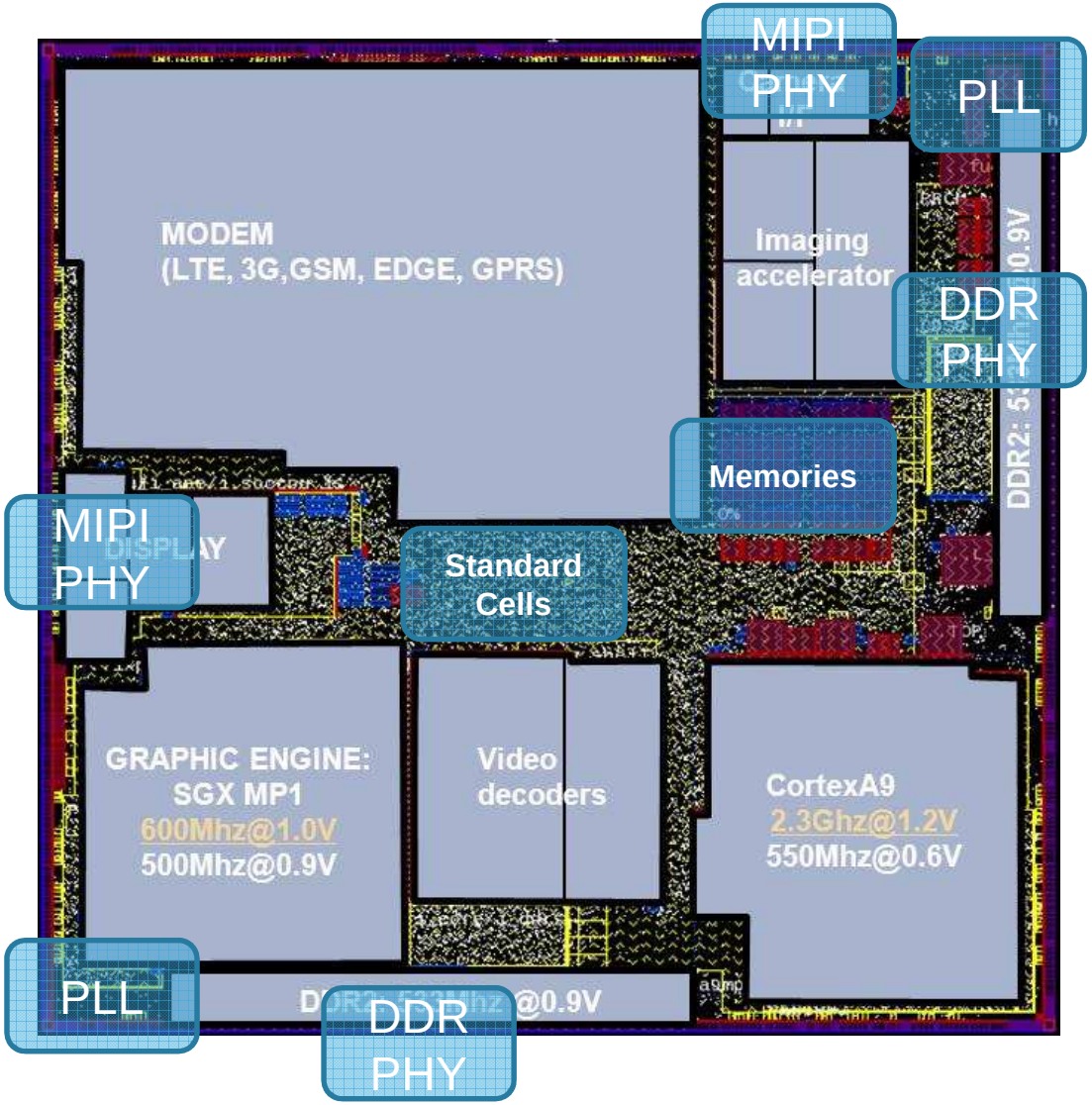
System On Chip (SOC) contents

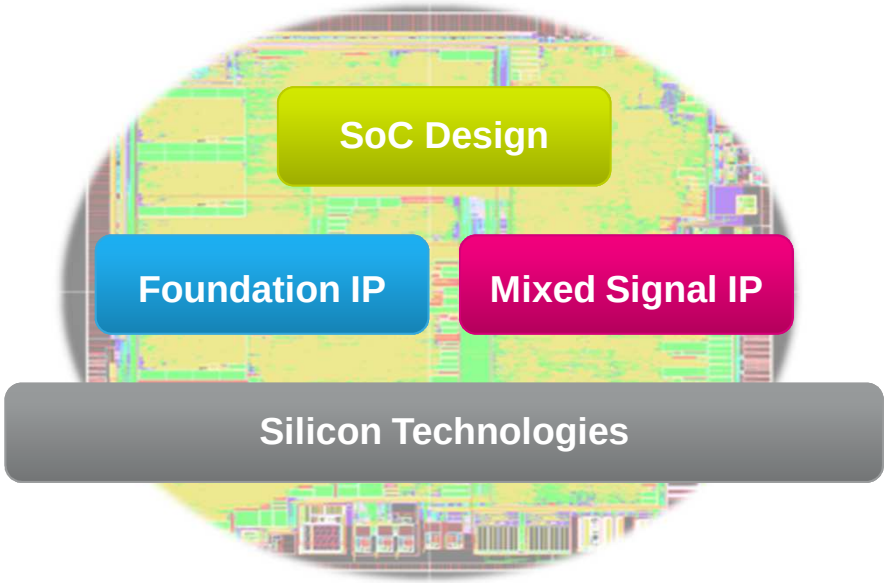
- SoC made of :
  - Array of standard cells
  - Hard IP.
- Hard IP include :
  - Fundation blocks such as Memories, Standard Cells and IO
  - Complex mixed signal IP such as High Speed Serial and Parallel Interface.



IP development challenges

Foundation Libraries

- Digital Logic Cells
- IOs & Fuse
- Embedded Memories
- Testability & Repair Solutions



Analog & Mixed signal IPs

- Clock Generators
- Data Converters
- Interfaces PHY
- RF & Power Management IPs

From AMS IP perspective, SoC Silicon success relies on :

- Agility to design IP (specs refinements, productivity, robustness,…)
- Matching between hard IP model and electrical characteristics
- Accuracy of models representing IP (stdcells, memories, hard IP,…) in digital flow
- Predictability of electrical characteristics

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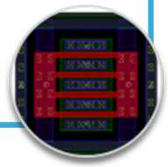
Full Custom Flow Ecosystem

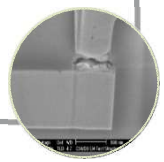
PDK

- Libraries
- PCells
- Rule decks
- Stacks



Process

- Design Rules
- Lithography
- Spice models
- Reliability



Flow

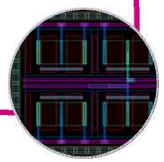
- Flow Definition
- Scripting
- Qualification

Infrastructure

- Deployment
- Documentation
- Trainings
- Support

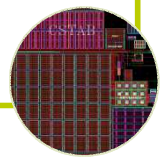
EDA Vendors

- Collaboration
- Co-developments

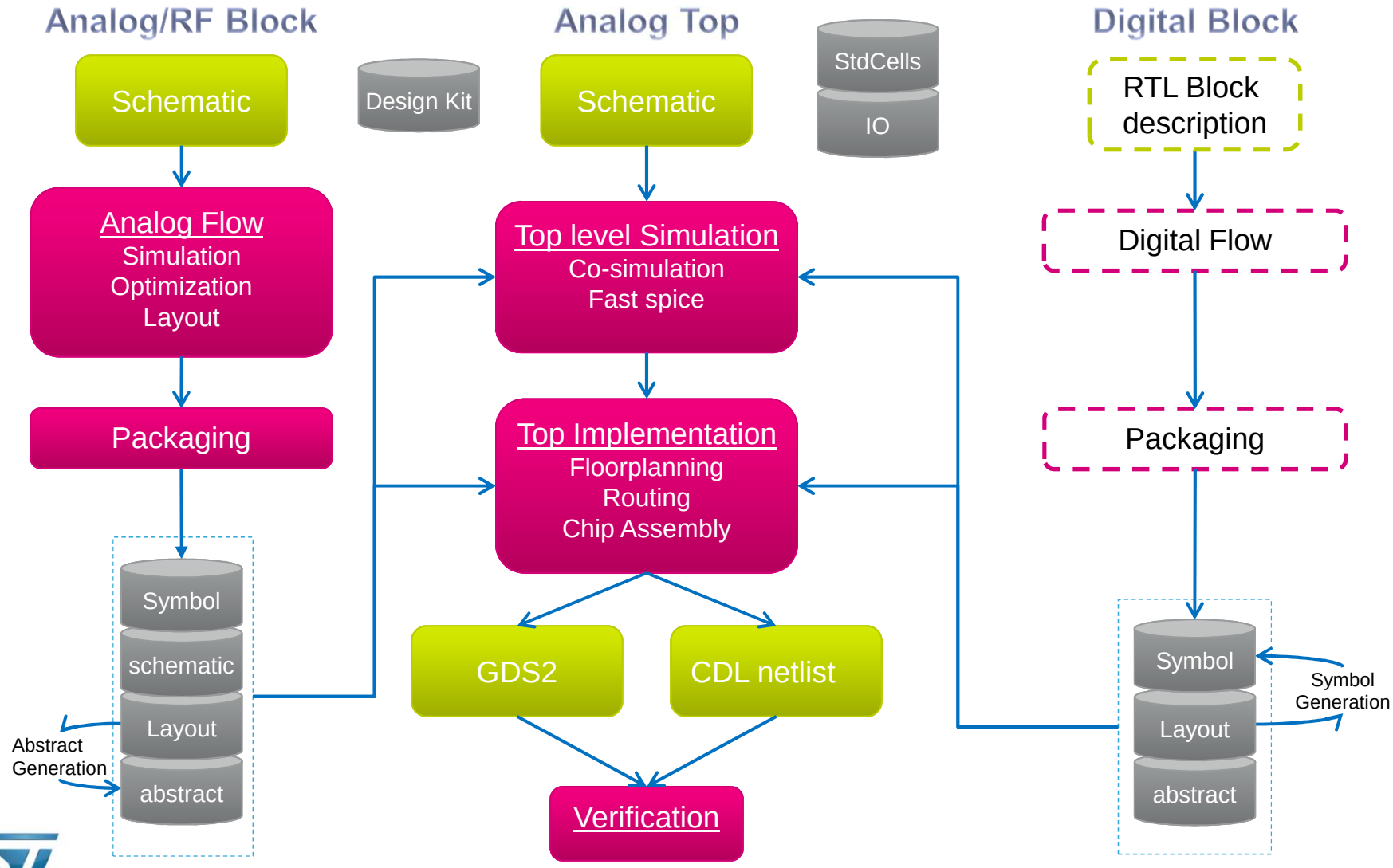


Designers

- Flow definition
- Early adopters
- Testchips



Analog RF IP Design Flow - Summary



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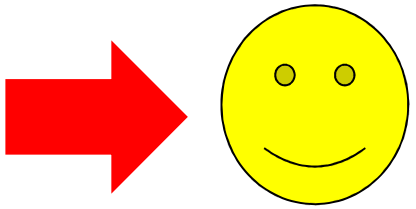
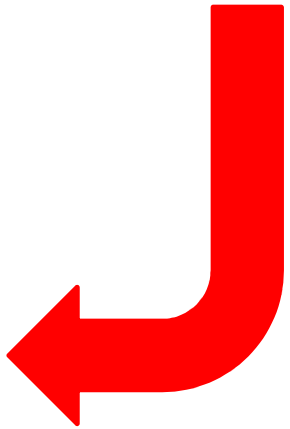
Analog design basic assumptions

Full custom design axiom
You get what you simulate





- Analog designer will always concentrate on schematic improvement…
- Simulation predictability remains the fundamental of full custom design!

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But….

Is full custom designer confident enough to commit on First Time Silicon Success?

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Digital world : going further in Project Automation

Compute farm

Storage

CAD Tools

Libraries / IPs

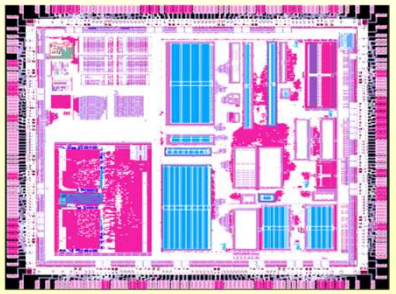
Design Flow

Scripts

Analytics

Reporting

Defect management



Design decisions

Execution

Database management

Integrated design management

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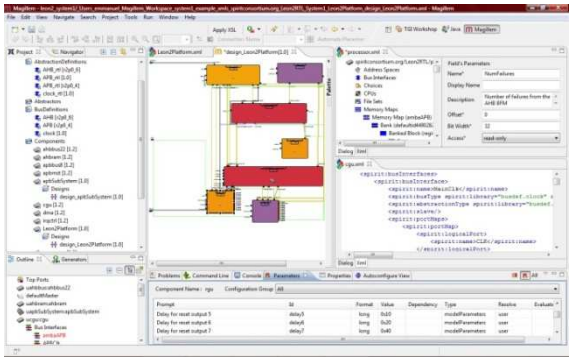
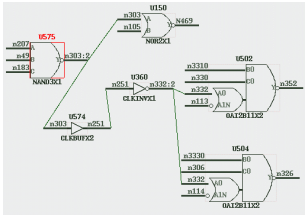
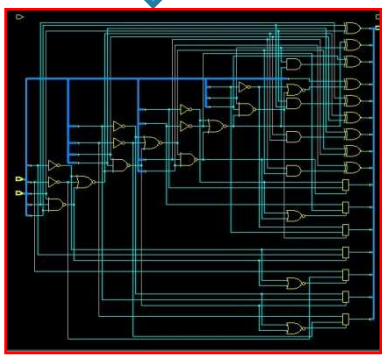


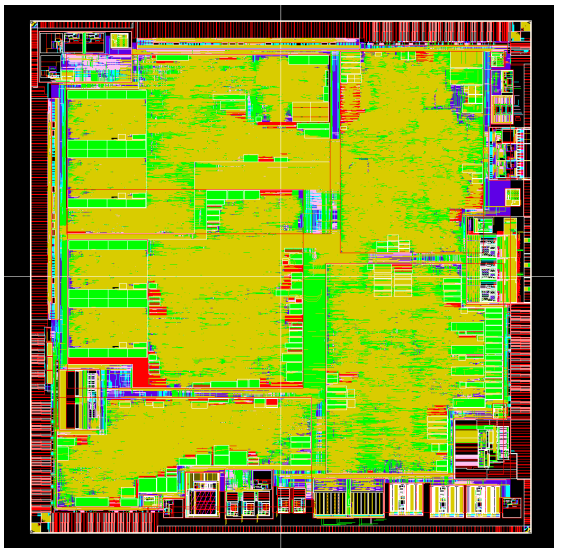
Programming language or symbolic representation of hard macro



Hierarchical view with macro function



Synthesis based on Standard Cell libraries and Memory model



Automatic Layout generation

EDA tools have enabled SoC design hidding technology complexity by high level of abstraction and use of macro models.
Binary coding and Bolean description were key ingredients.

Digital world : programming language and scripts

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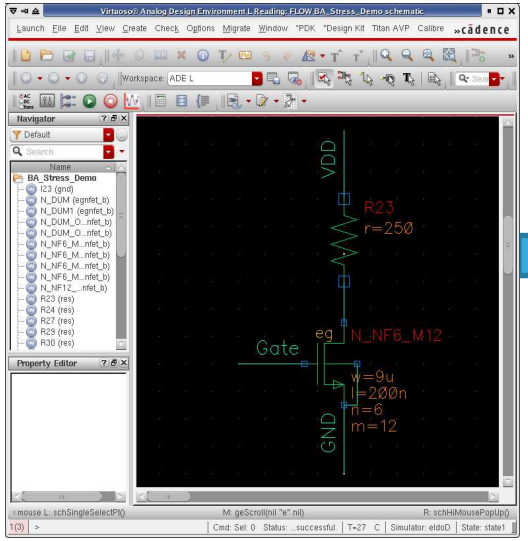
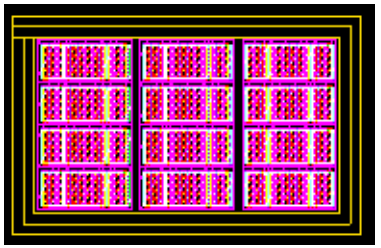
Full custom world… a device world

Full custom design relies on a very large database of proven schematics which are adapted to Si process specificities.

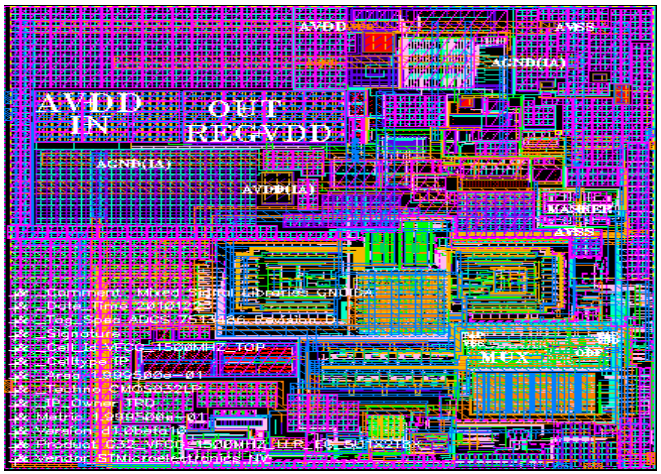
Key enablers for fast and predictable solutions are model predictibility and simulator speed.



From schematic to basic layout device



Transistor level assembly and connection routing



Extraction of parasitic and layout effects

Back annotation : Addition of parasitics to schematic

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Snapshot of Si experience in 28nm node

IP Type	Problem Description	Product Impact
FUSE	IP not working at nominal value but below vdd min	Blocking, functionnality issue
FUSE	Degradation of bit reading efficiency	Relability issue
High Speed Interface	High Speed Link Loopback failures	DFT issue
High Speed Interface	Skew between input signals leading to high BER	Performance limitation
IO	Very high loading leads to high transient consumption and bump on the supply	Performance limitation
IO	Input Leakage around +200uA observed at IO pins where internal pull-up/pull-down is enabled causing external on board pull-up or pull-down not to work	Performance limitation
IO	IO Compensation block out of spec	Blocking, functionnality issue
ADC	If complementary input is applied at two channels of ADC then the performance of input-2 is degrading.	Performance limitation
ADC	With active high impedance input of channel-I of DAC, the output of channel-Q is also in high impedance mode.	Blocking, functionnality issue
DDR	DFI Init start not working	Blocking, functionnality issue
DDR	Non functional behaviour at low fequency	Performance limitation
Power Management	Power switch not working in certain power supply configuration	Performance limitation
Power Management	Internal voltage reference out of spec	Performance limitation
Power Management	Output voltage limitation	Performance limitation

- Performance limitation is major consequence of non performing AMS IP
- Missing functionality still remains a major issue

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Root cause analysis

IP Type	Root cause analysis
FUSE	Functional simulation coverage
FUSE	Fab dependence, sense amplifier sensitivity
High Speed Interface	Functional simulation coverage
High Speed Interface	User specification definition
IO	Use case not covered
IO	Use case not covered
IO	IR drop
ADC	Cross talk
ADC	Functional simulation coverage
DDR	Functional simulation coverage
DDR	Use case not covered
Power Management	Use case not covered
Power Management	Electromigration
Power Management	Connection through well

- Specification definition and use case description is the main root cause of failure.
- Functional and performance simulation coverage is consquently the second cause of failure

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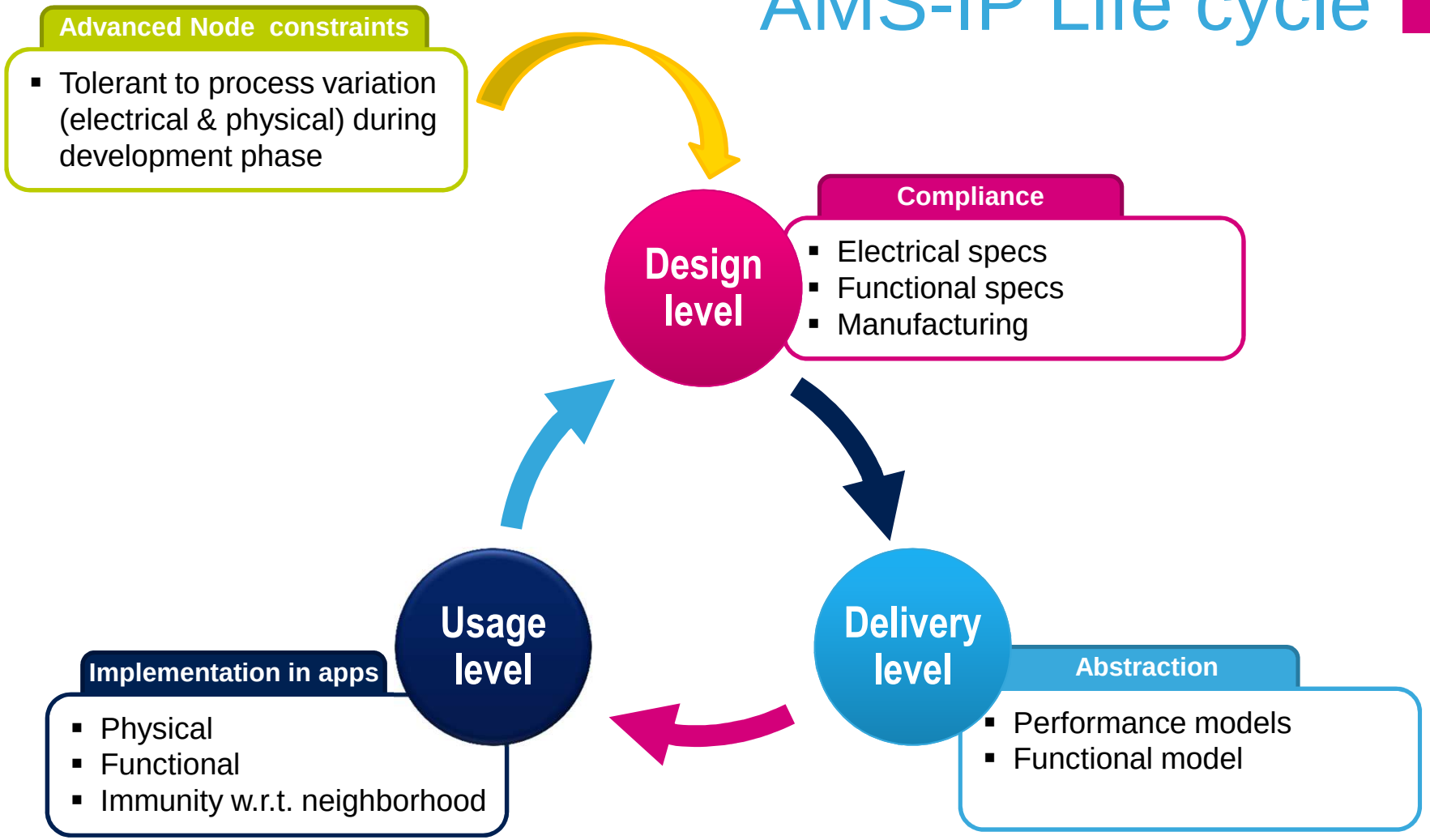
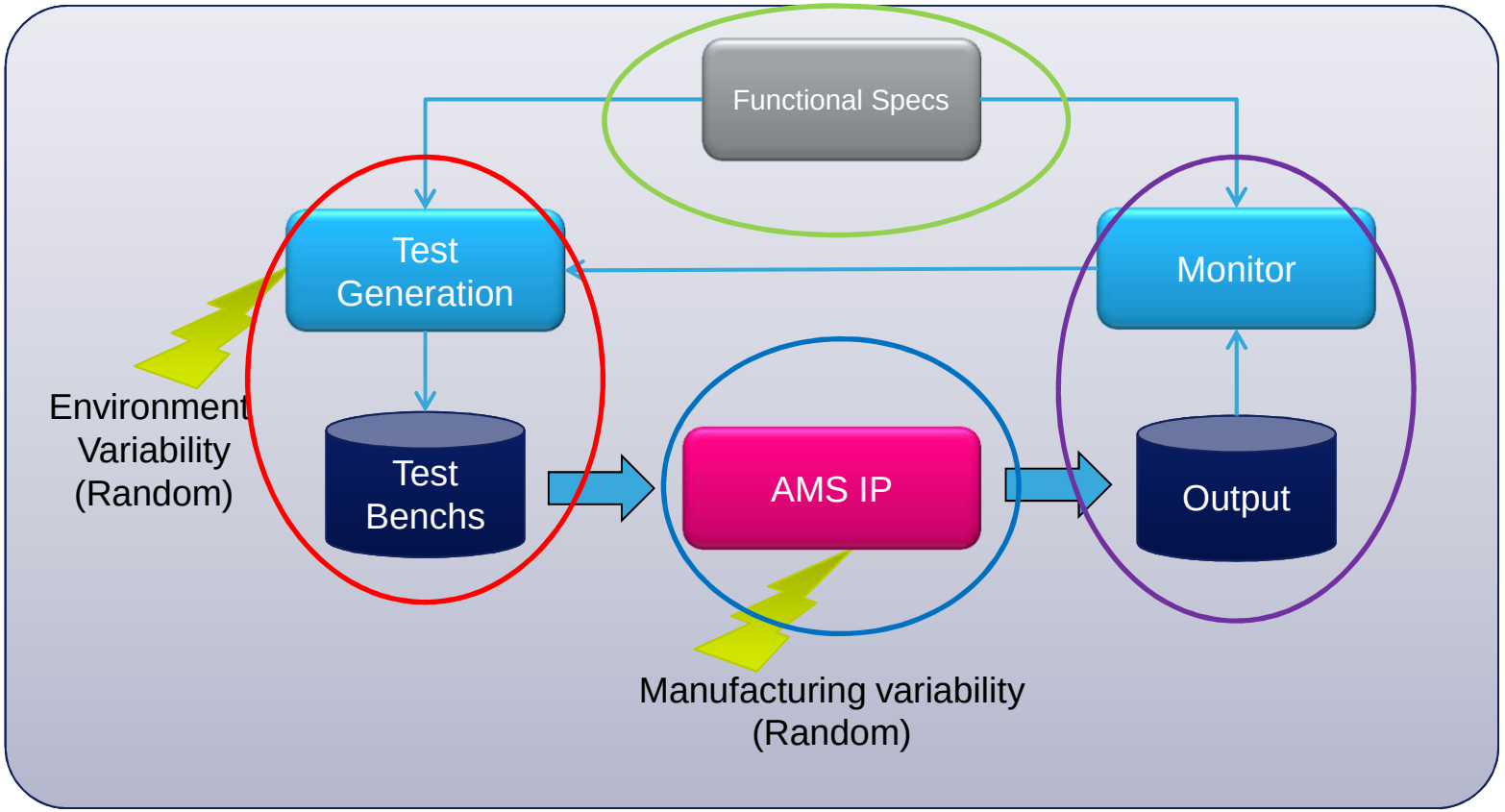
AMS-IP Life cycle



AMS IP Verification - Challenges



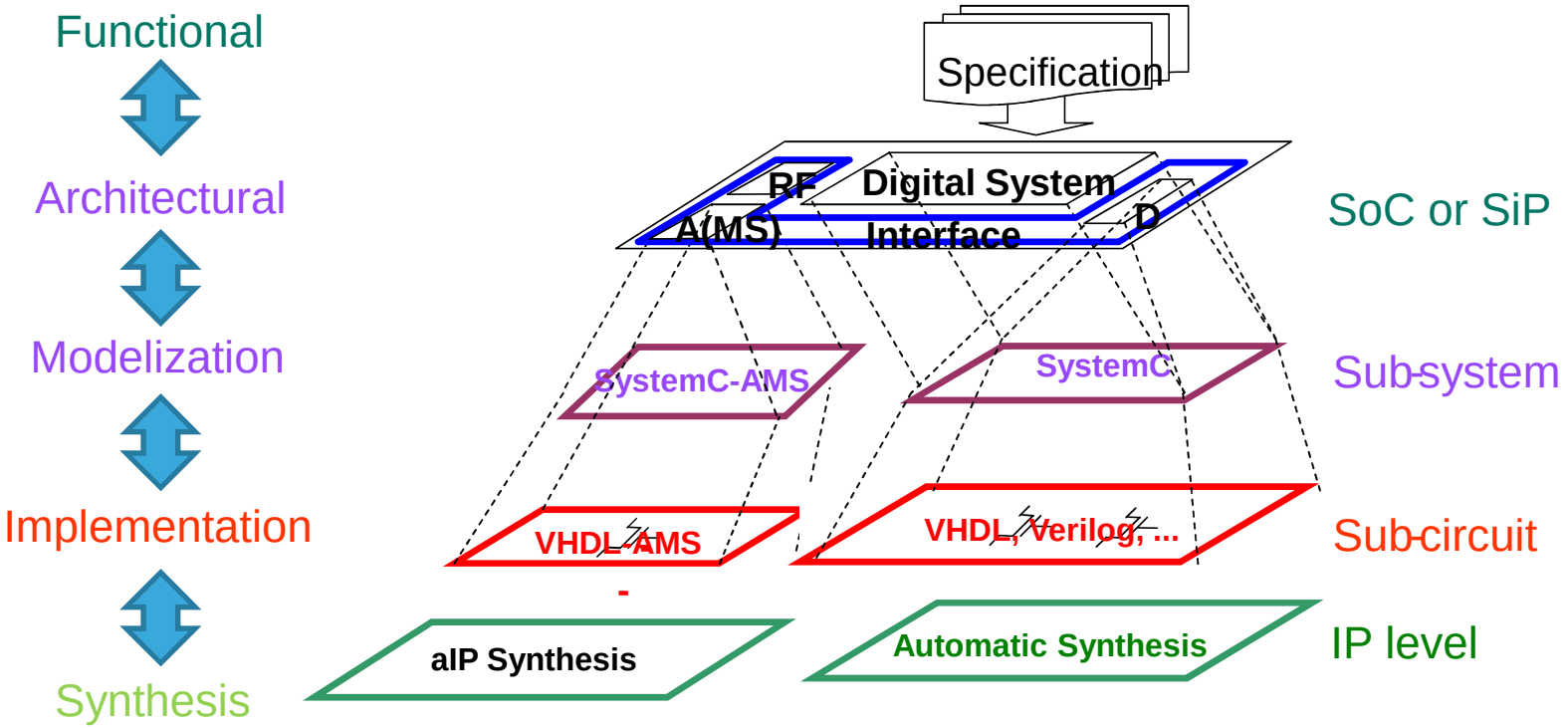
Specification definition

Tests definitions / execution

Block abstraction

Results analysis & Coverage

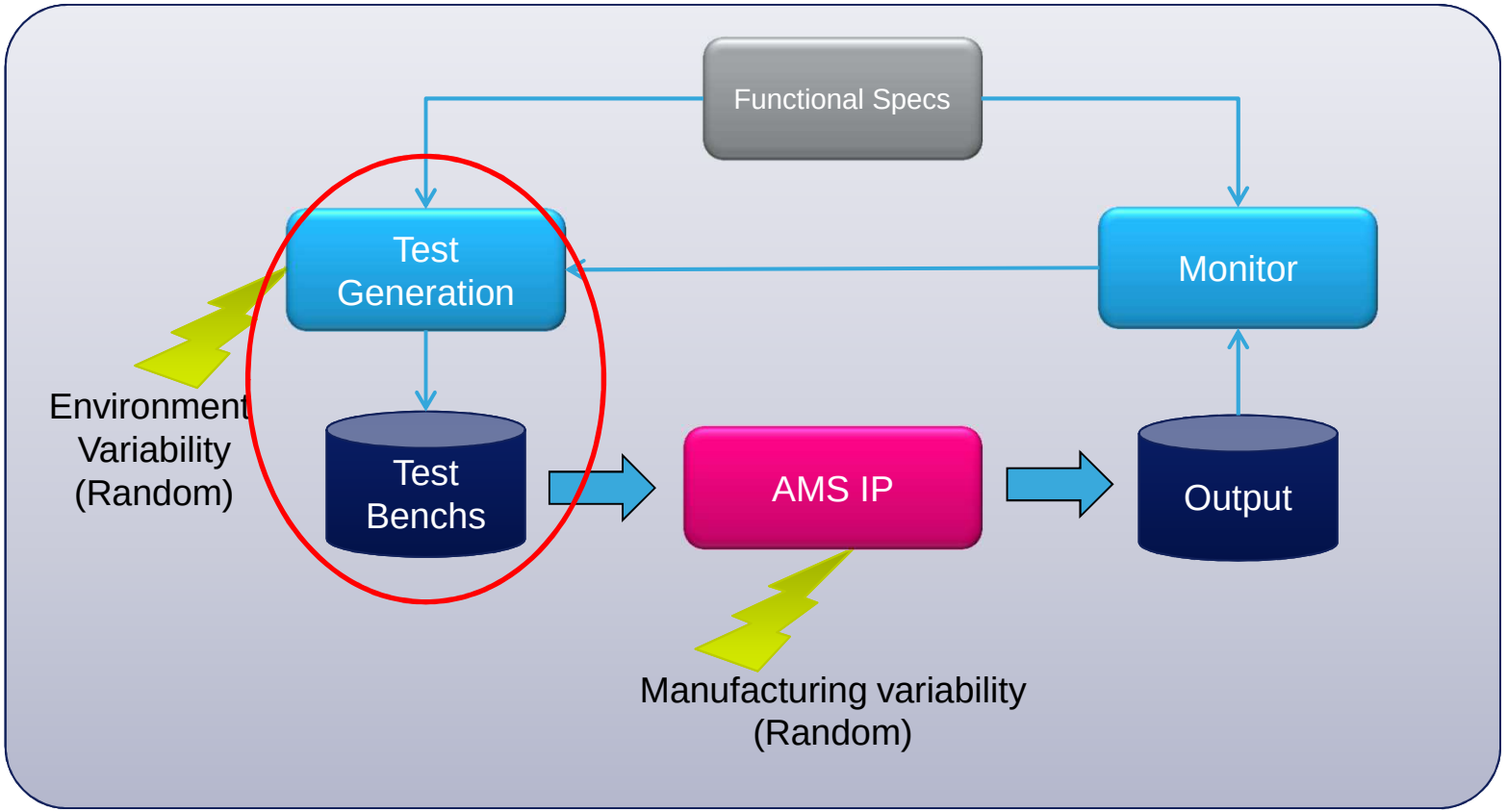
Pb0 : Functional specs definition



Need to change cultural approach for analog design community :

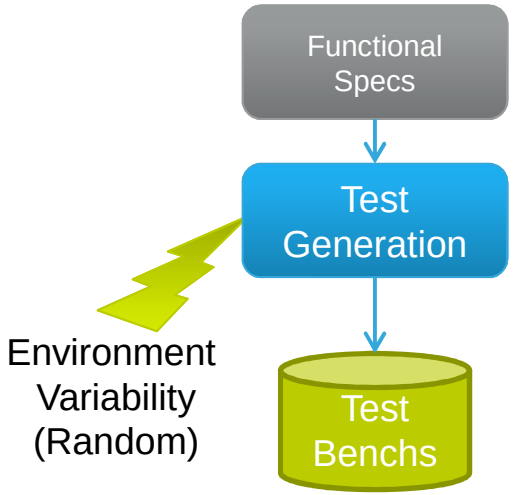
- Move from “bottom-up” approach to “top-down” approach
- Develop “user friendly” tools

AMS IP Verification - Challenges



Tests definitions / execution

Pb1 : Tests definitions / execution



Geometric

- Manufacturability

Require geometry / connectivity

Dynamic

- Timing / power
- Variability : output spread
- Sensitivity to manufacturing & environment
- Thermal behavior
- Random effects (jitter,…)

+ Plus input vector & **costly** simulations

Static

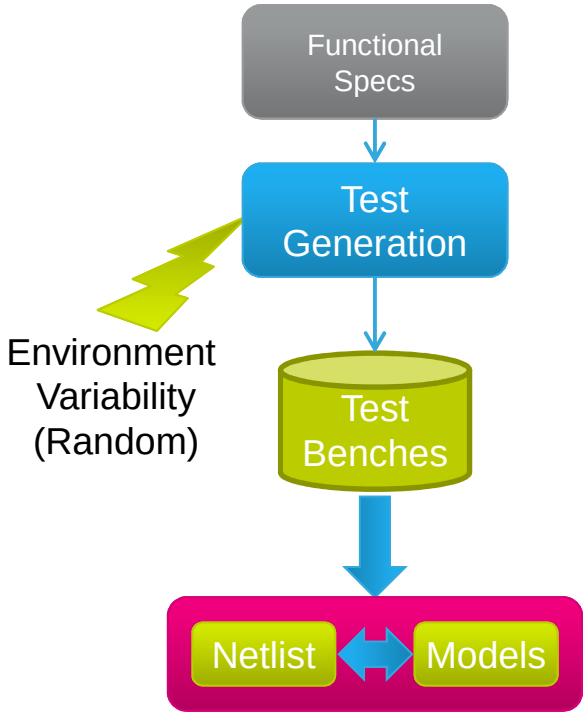
- Power domain compliance
- ESD compliance

+ Usage information / context

Need to build theories/methodologies to :

- Transfer functional specifications into test benches and stimuli
- To emulate fault vector/benches to cover unexpected events

Pb 2 : Simulation time and models

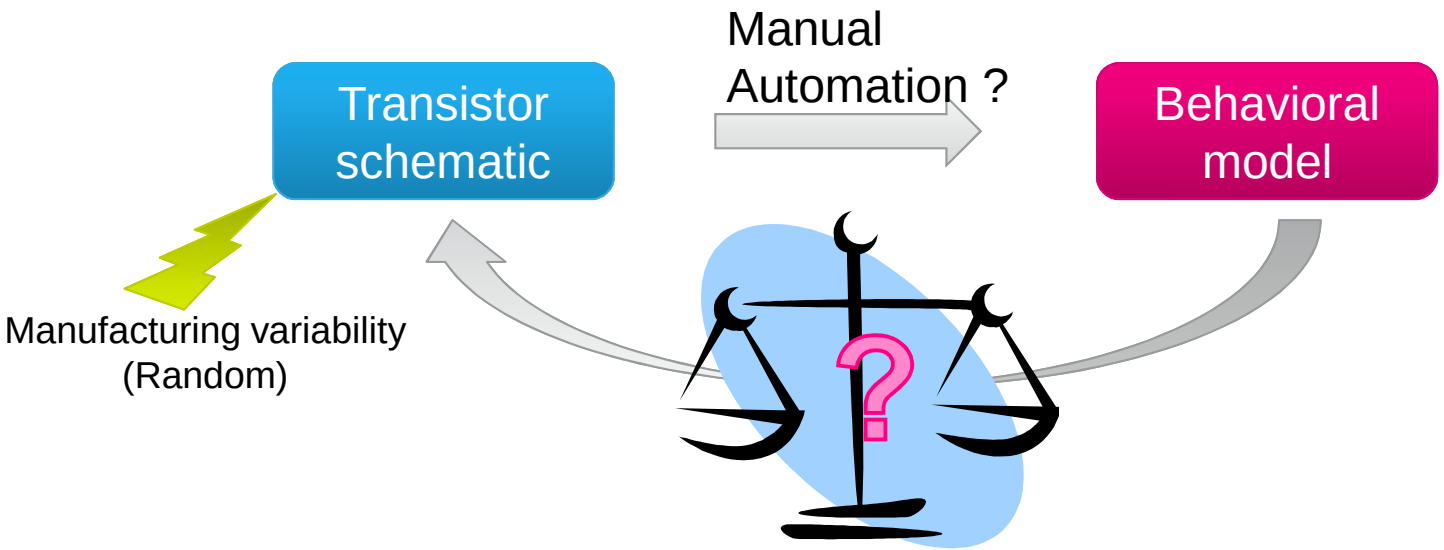


Test vector and test benches usage :

- Netlist simulation are often inadequate to cover the full set of test benches and stimuli
- Higher level of abstraction is requested to be able to insure sufficient test coverage

Pb2 : block abstraction

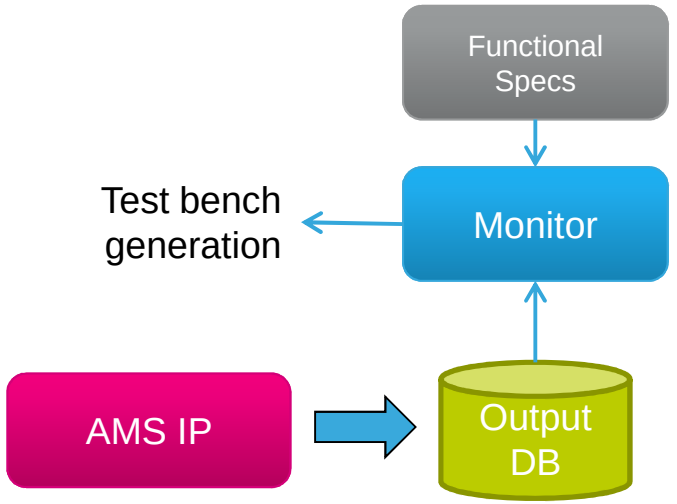
- Purpose of the model : timing , power, thermal, functional,…
- Validity domain: certification & check
- Functional / Failure mode
- Process / Environment variability



At which **confidence level** can we guarantee the equivalence between the behavioral model and the transistor view ?

Pb3 : Check and monitor

- Dynamic checks during simulation:
  - Reliability checks / Operating regions
- Formal waveform analysis
- Comparison with specifications



☹ Lack of standard language

☹ Adoption by EDA industry (market share?)

☹ Reluctance to change by design community

☺ Advanced process require more and more reliability checks
→ Design community ask more formalism for verification

Standardization of pass/fail criteria in ad equation with functionnal and performances specification and test vector generation
Analog VIP development for standard based AMS IP (USB, HDMI, PCIe,…)

Analog verification : moving ahead

Analog community cultural change :
- Moving from “bottom-up” approach to “top-down” approach
- Development of tool friendly approach

Standardization approach :
- Translation of electrical parameters into stimuli generation
- Develop of analog VIP for standard based IP

Modelisation :
- Requirement of Mathematical approach to increase level of abstraction
- Formal proof of mathematical model versus IP netlist

Metrics :
- Definition of metrics for verification coverage
- Evaluation of sensitivity and risk analysis

While Si validation remains the today practice, predictability and verification of analog IP is becoming a must…… let’s address it!!